

### 4004 PROCESSOR INTERFACE



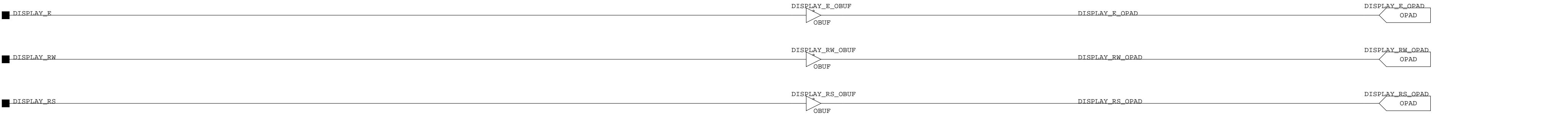
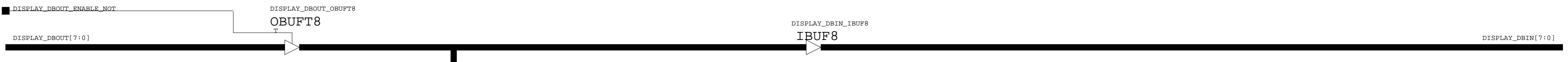
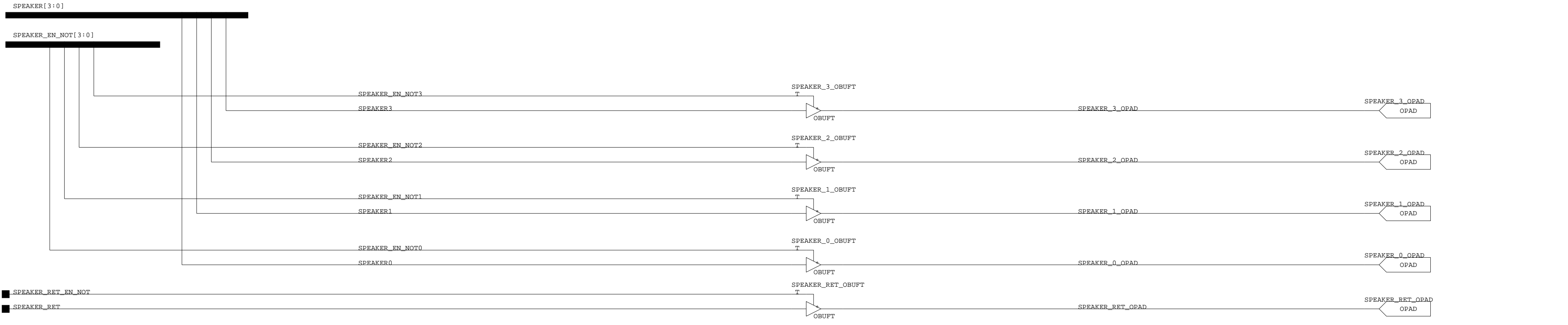
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Sheet Size: C	Rev:



### KEYBOARD INTERFACE



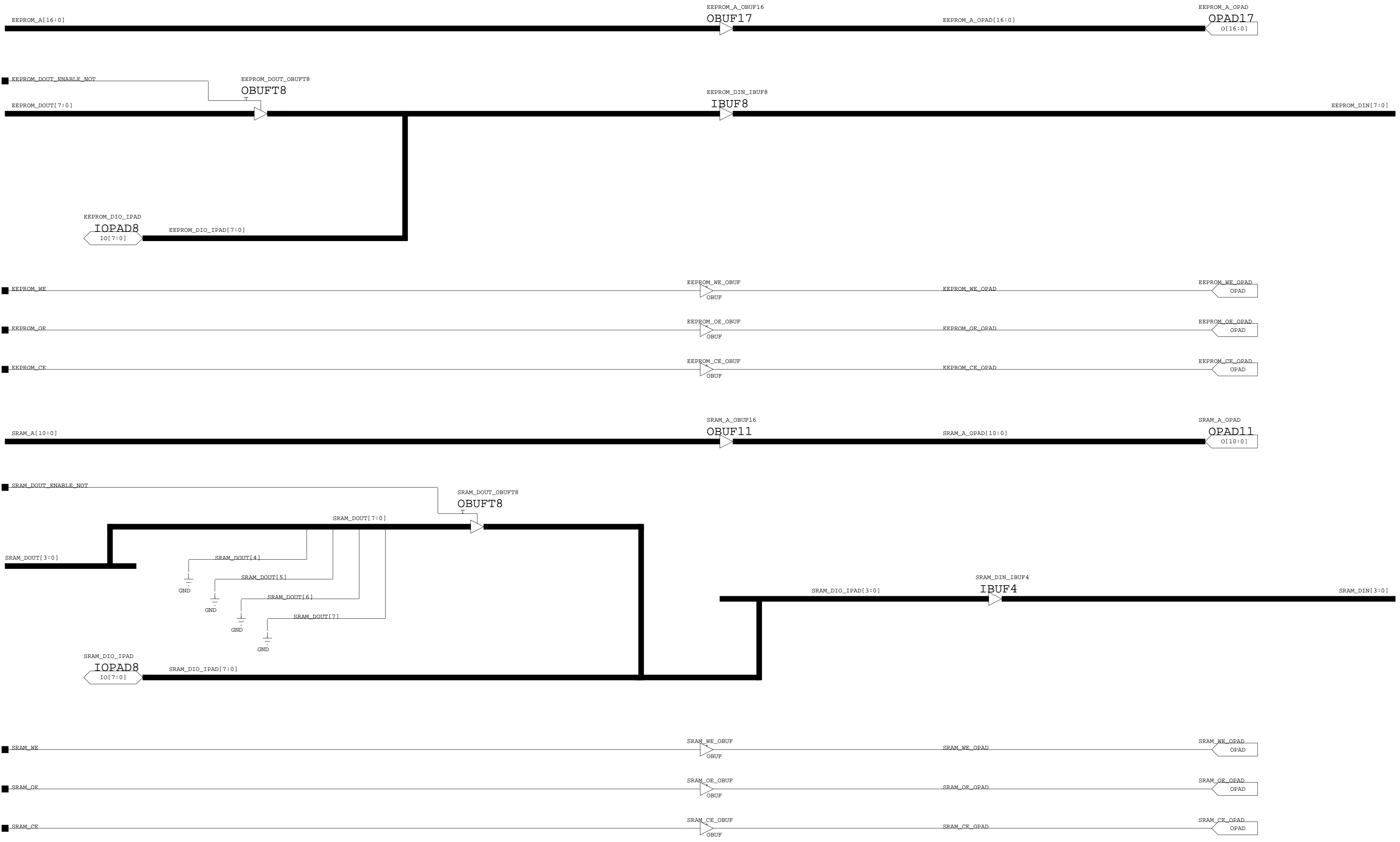
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Date: 3 OF 6	Ver:
Sheet Size: C	Rev:



SOUND/SPEAKER INTERFACE  
& DISPLAY INTERFACE



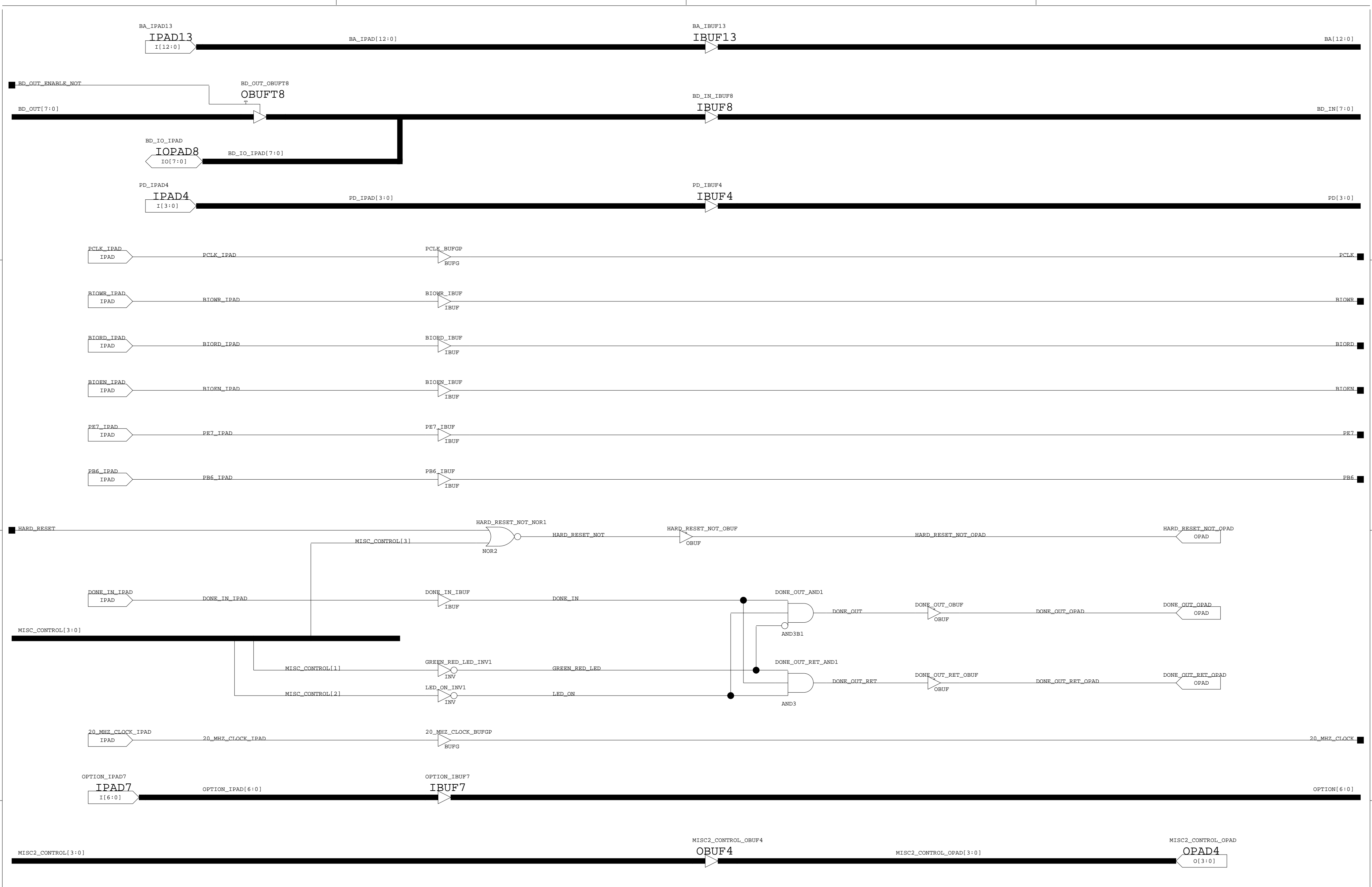
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Sheet Size: C	Rev:



### EEPROM & SRAM INTERFACE



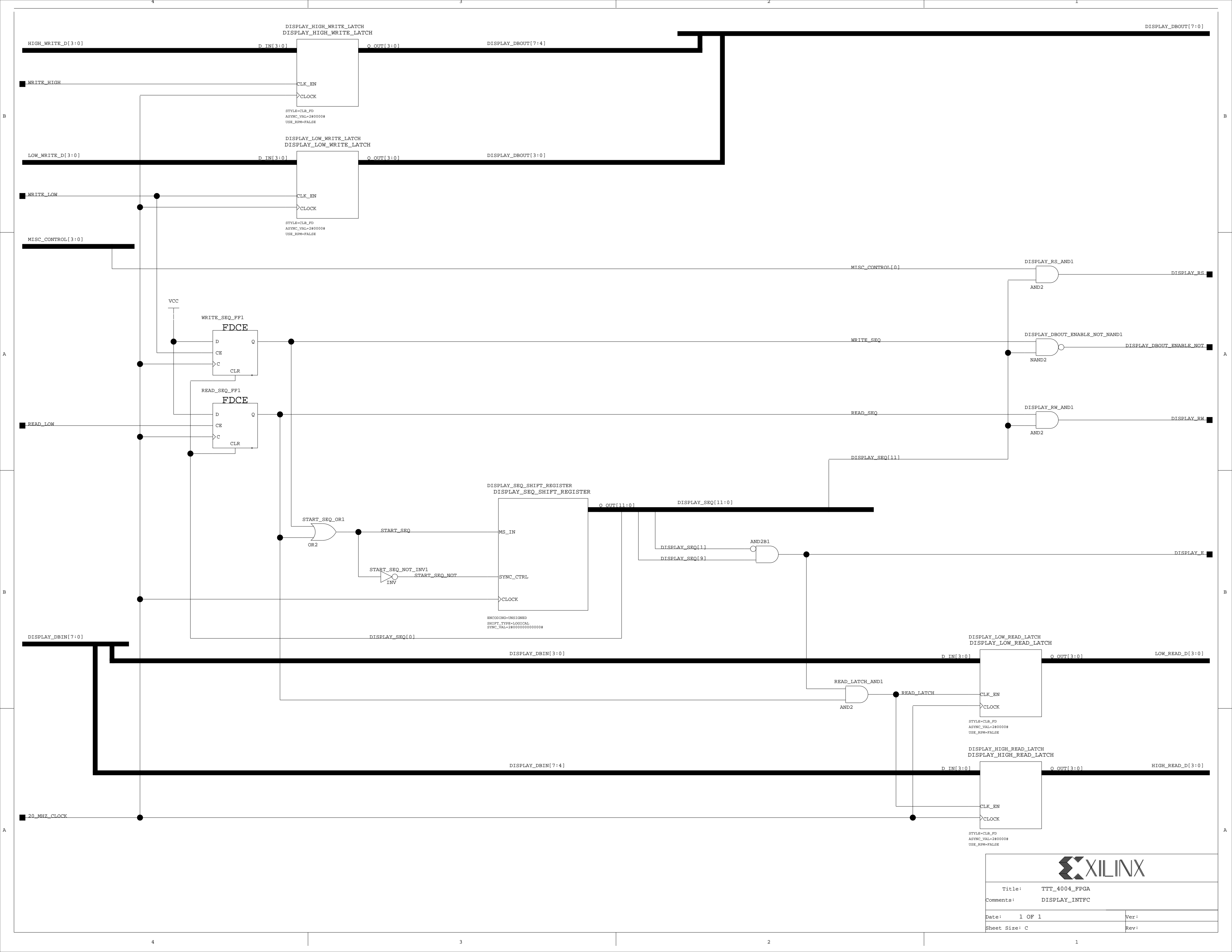
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Sheet Size: C	Rev:

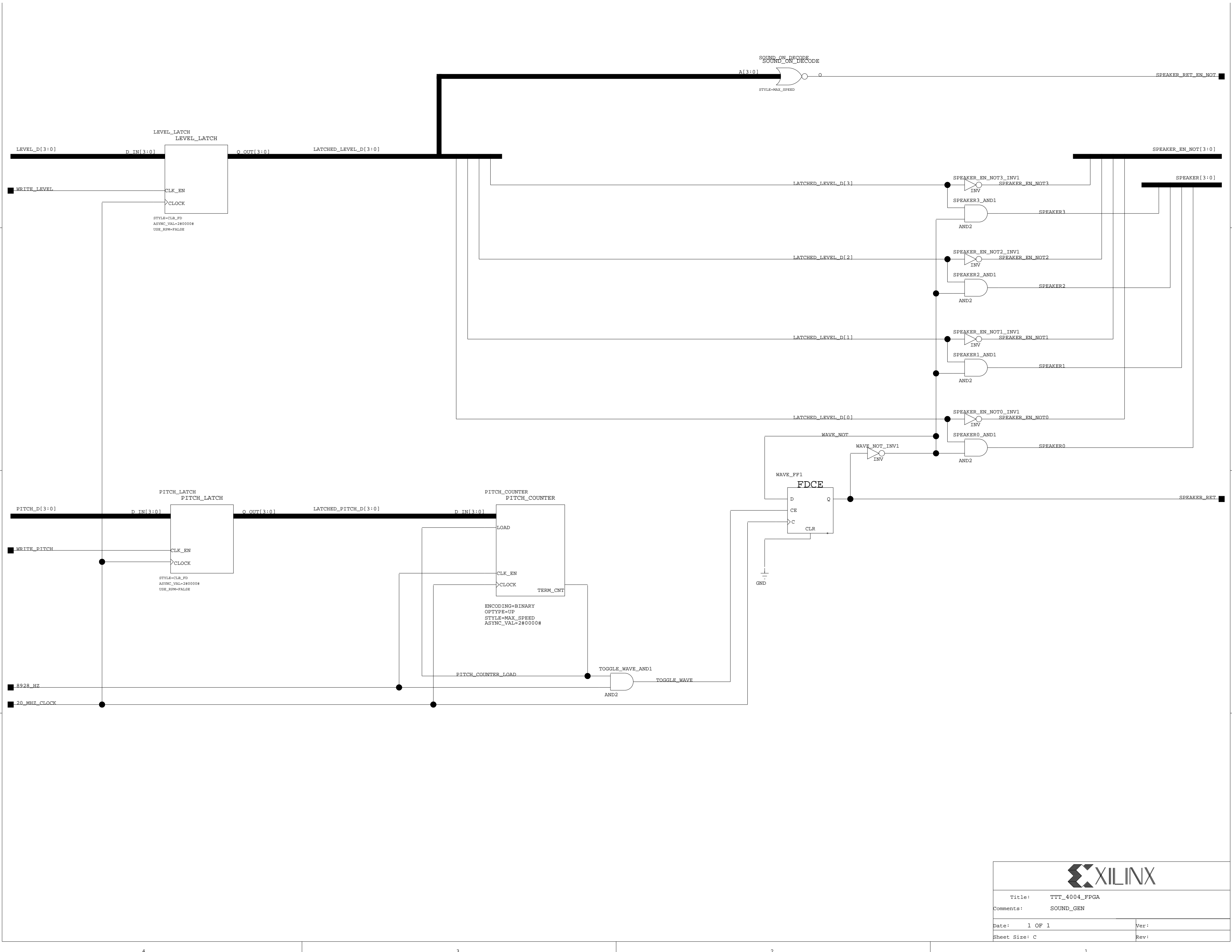


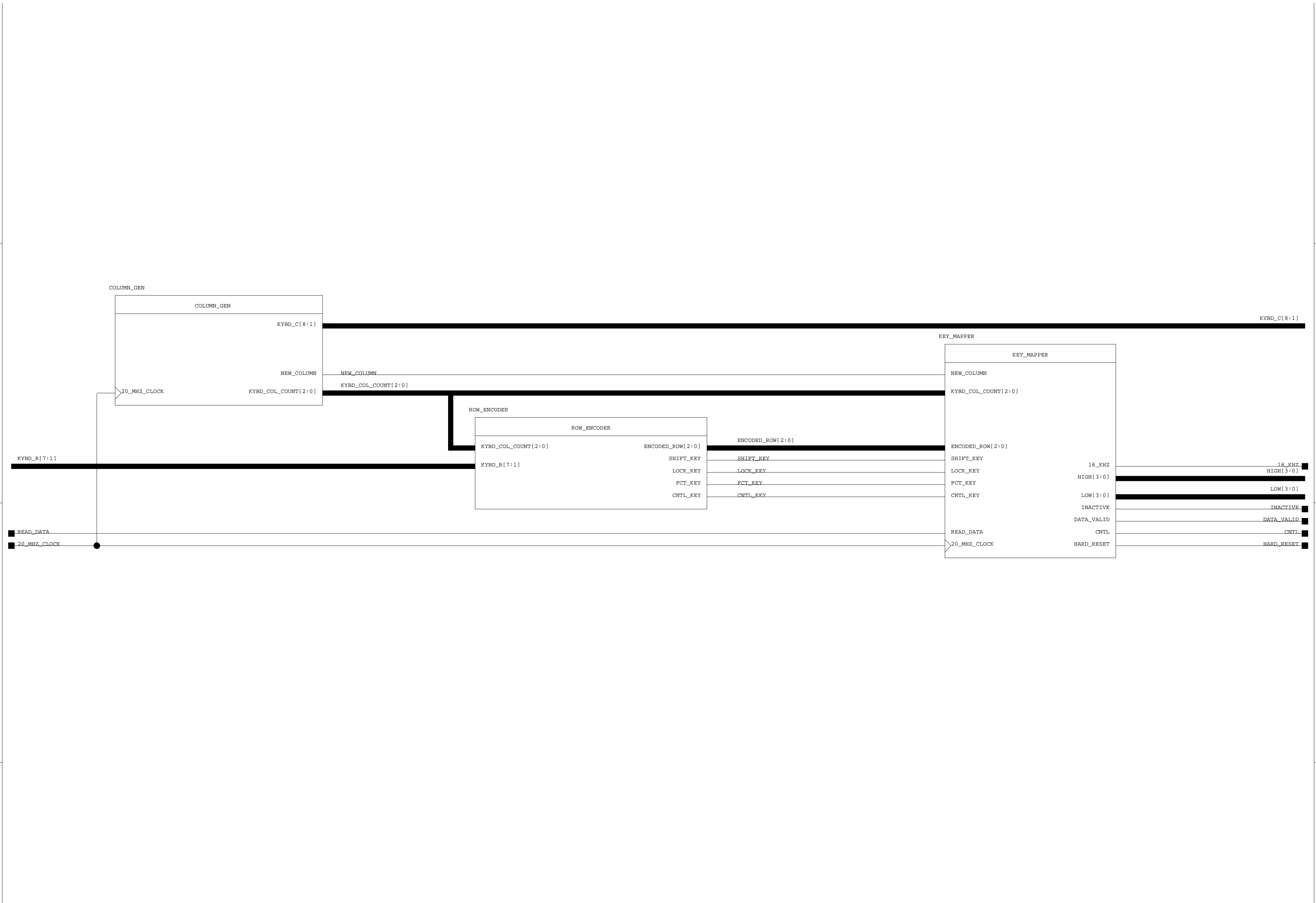
OPTION SWITCH, SYSTEM CLOCK,  
 DONE LED, HARD RESET INTERFACE,  
 MISC2 OUTPUT, & RABBIT INTERFACE

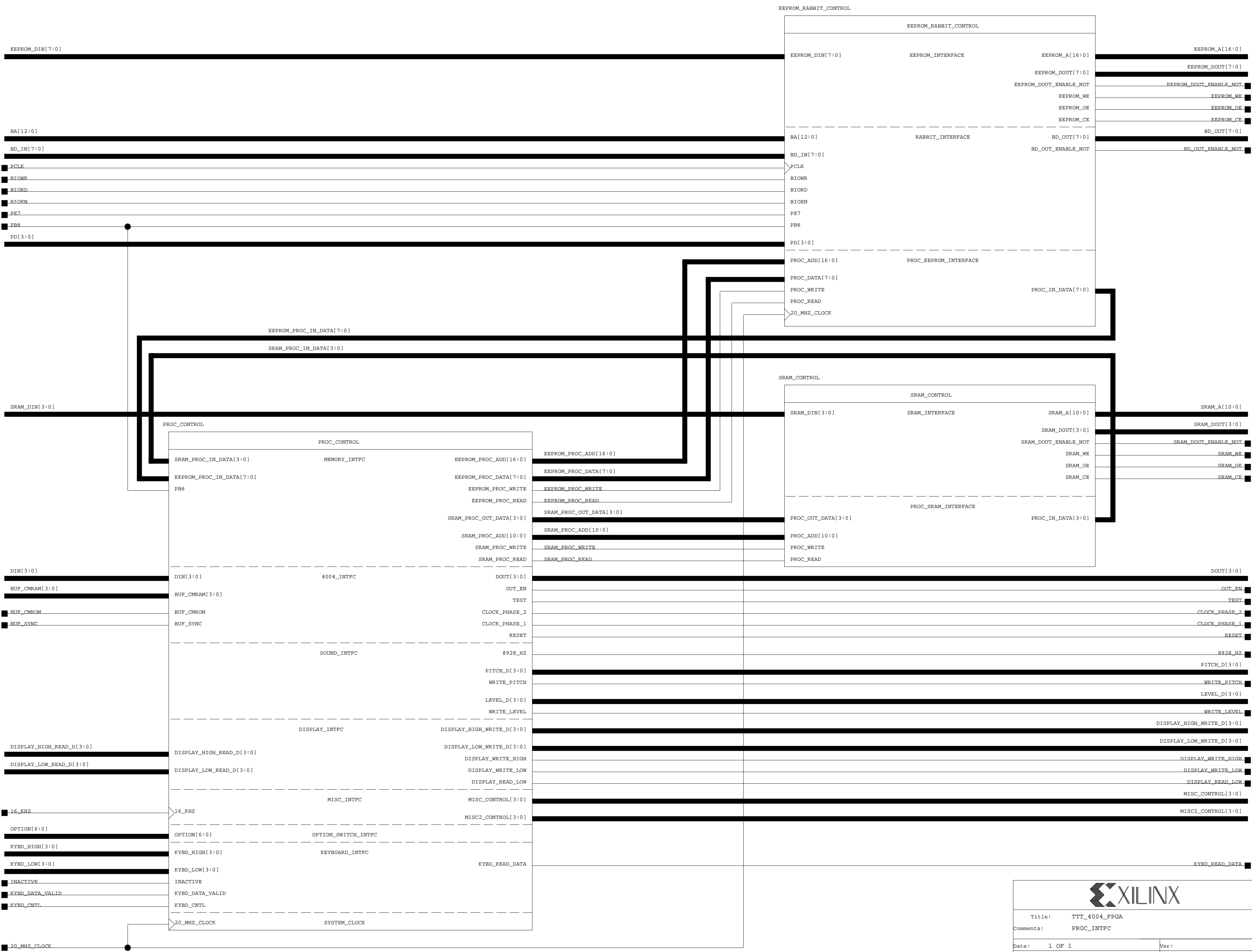


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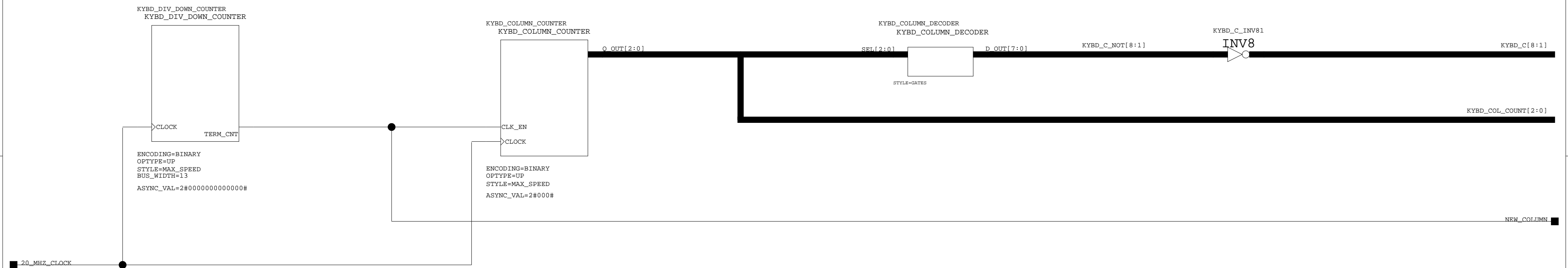




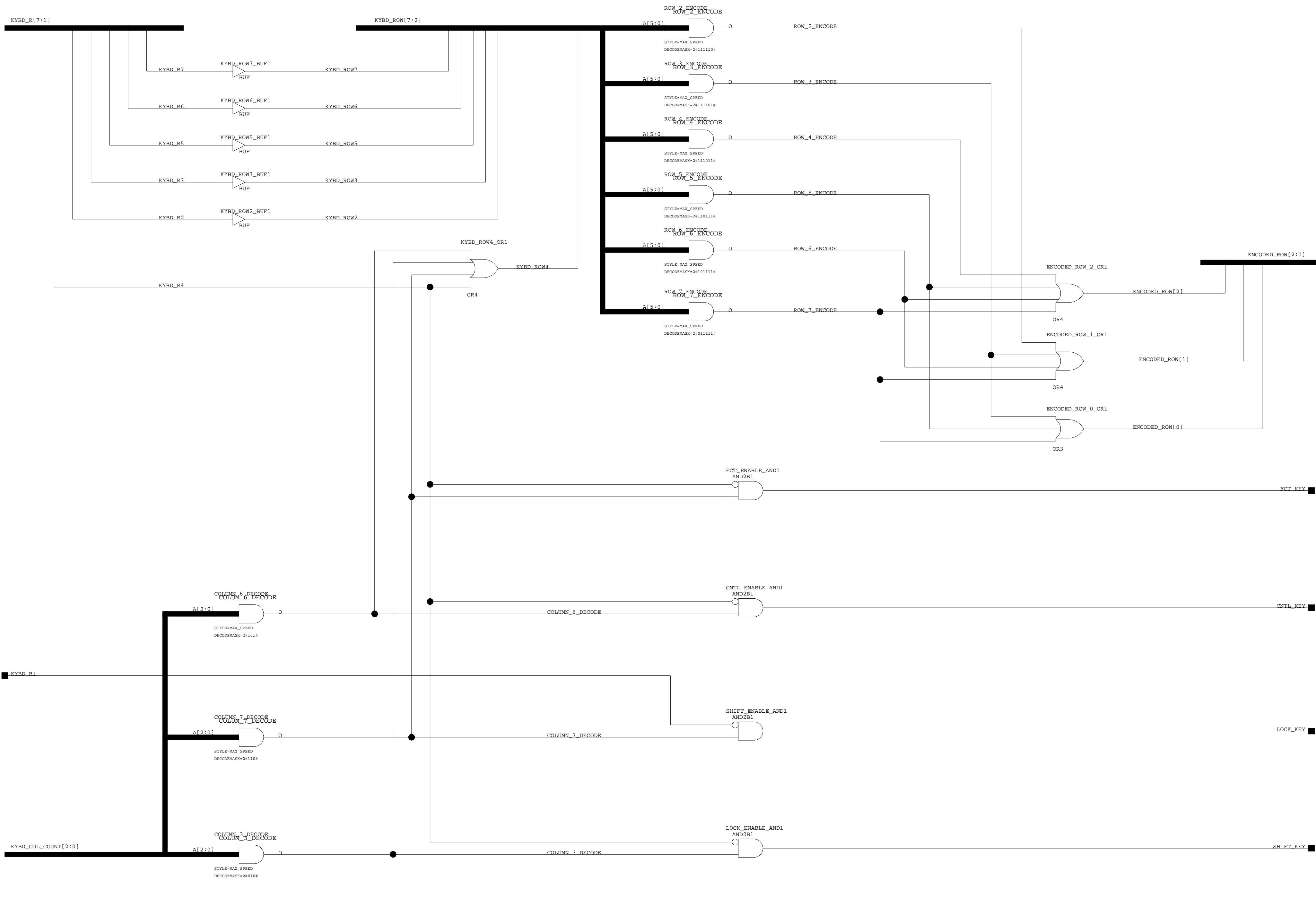


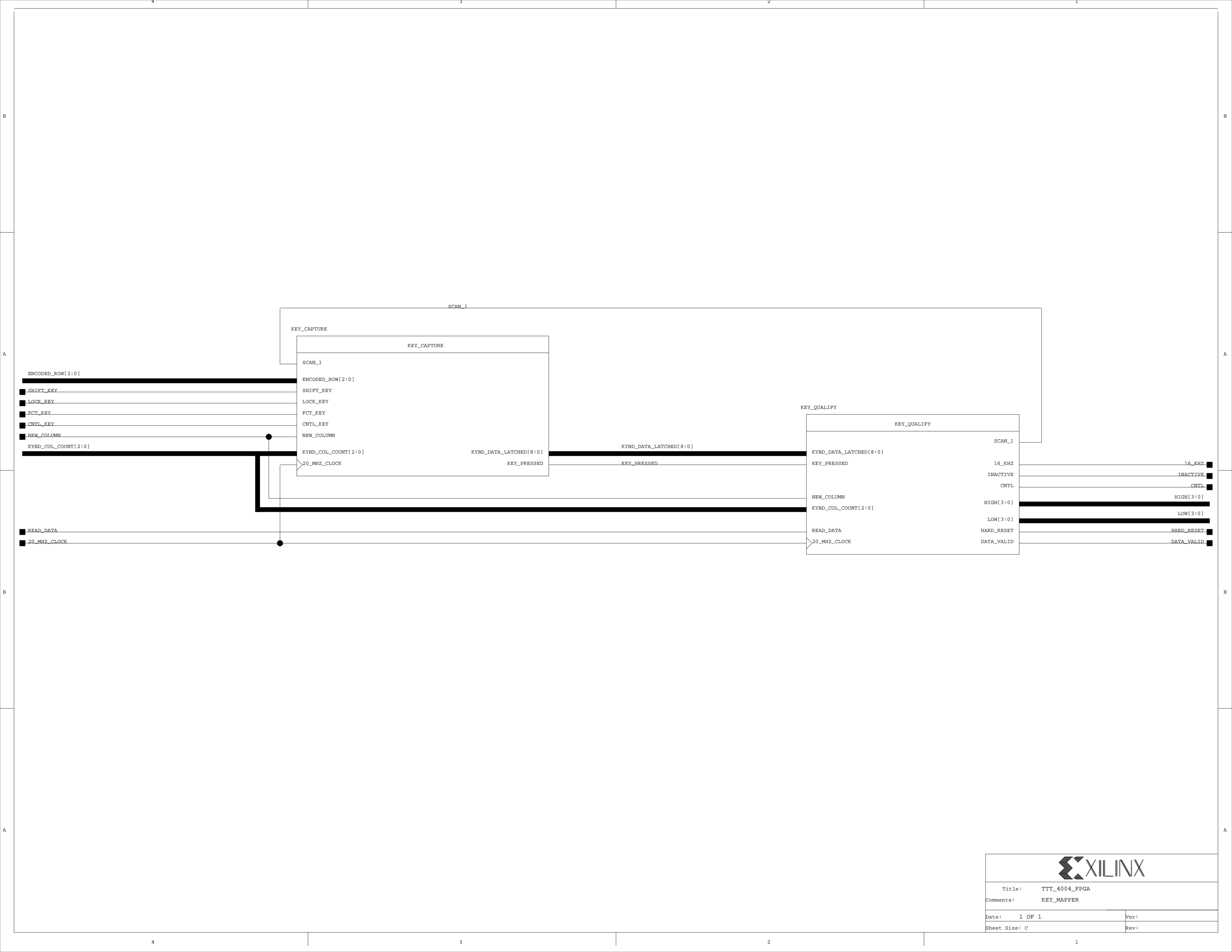


KYBD\_DIV\_DOWN\_COUNTER IS CHANGED FOR A LOWER DIVIDE DOWN RATIO FOR SIMULATION

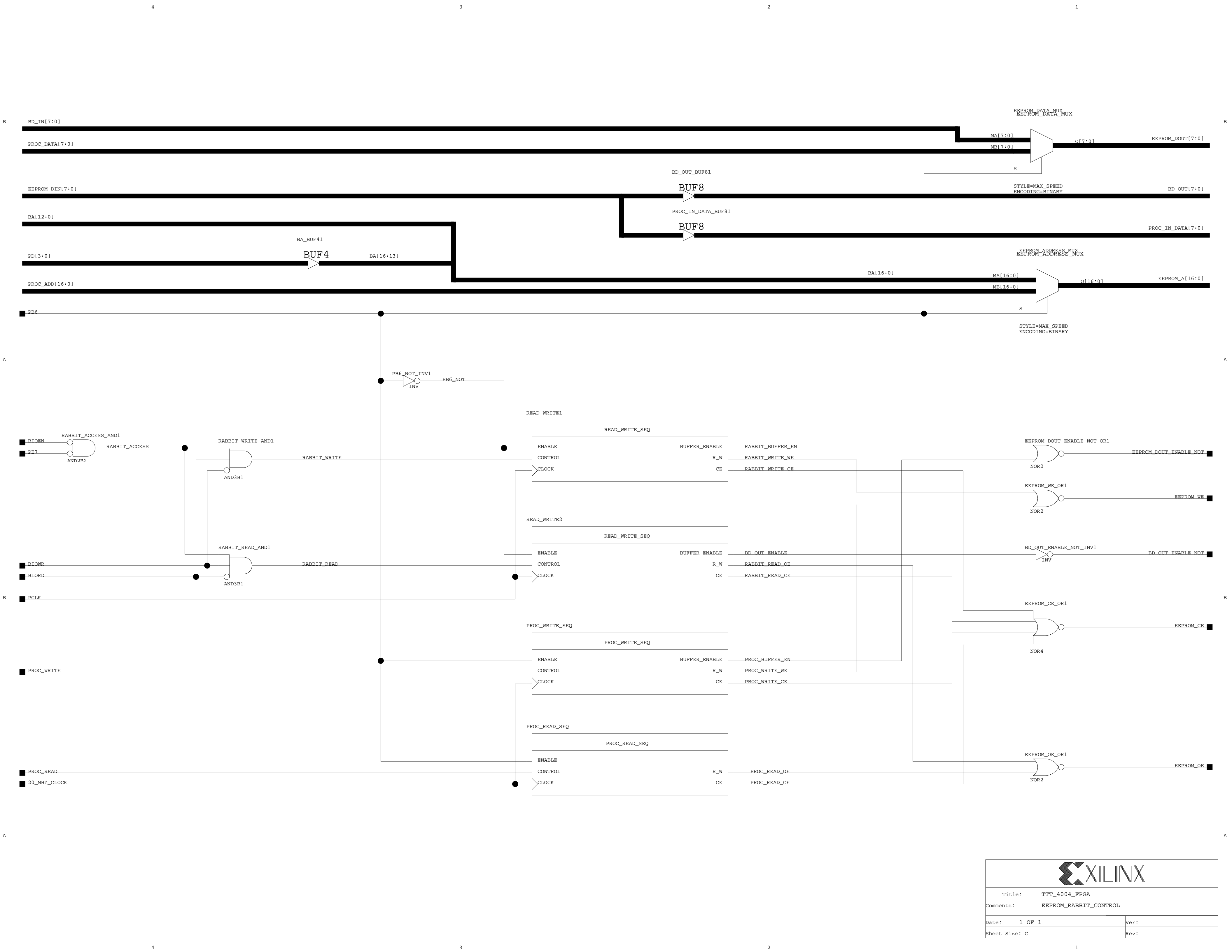


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Comments: COLUMN_GEN	
Date: 1 OF 1	Ver:
Sheet Size: C	Rev:





Title: TTT_4004_FPGA	
Comments: KEY_MAPPER	
Date: 1 OF 1	Ver:
Sheet Size: C	Rev:



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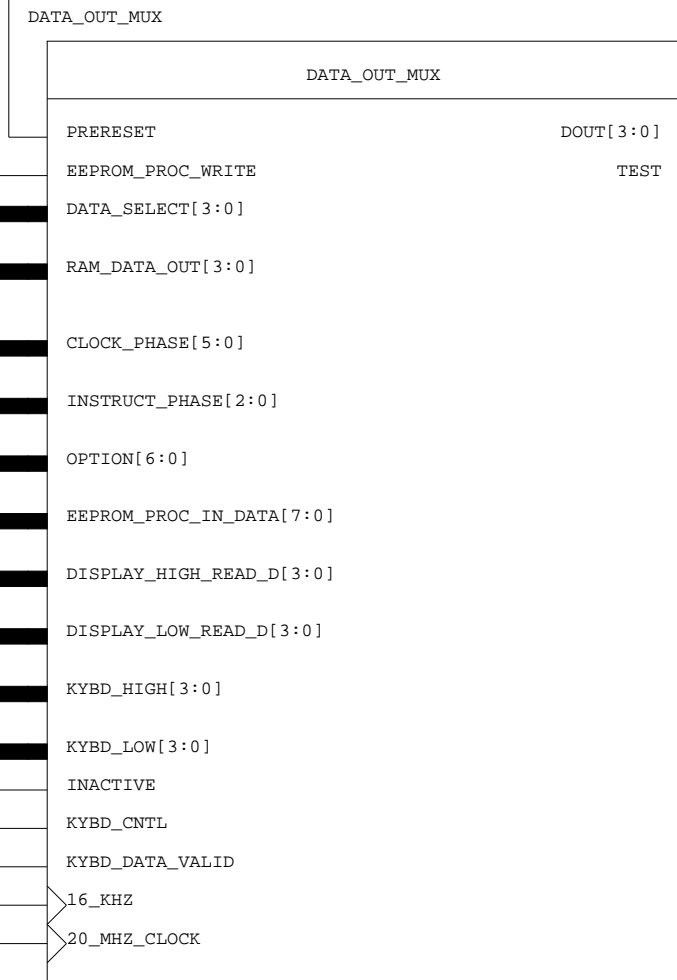
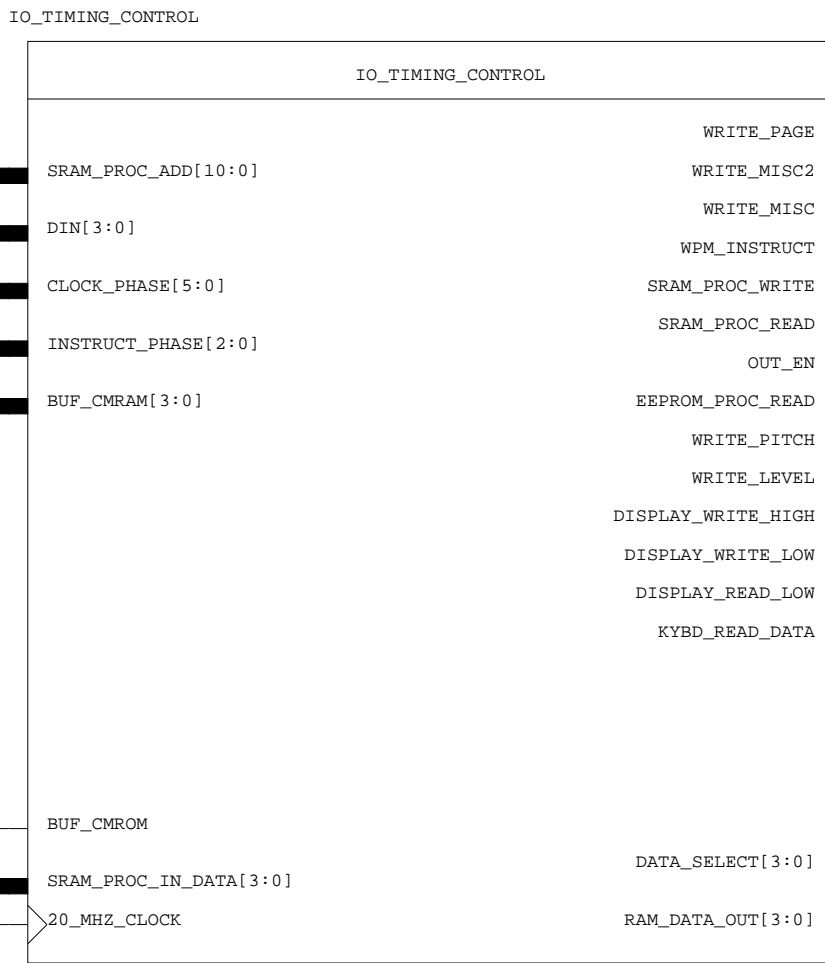
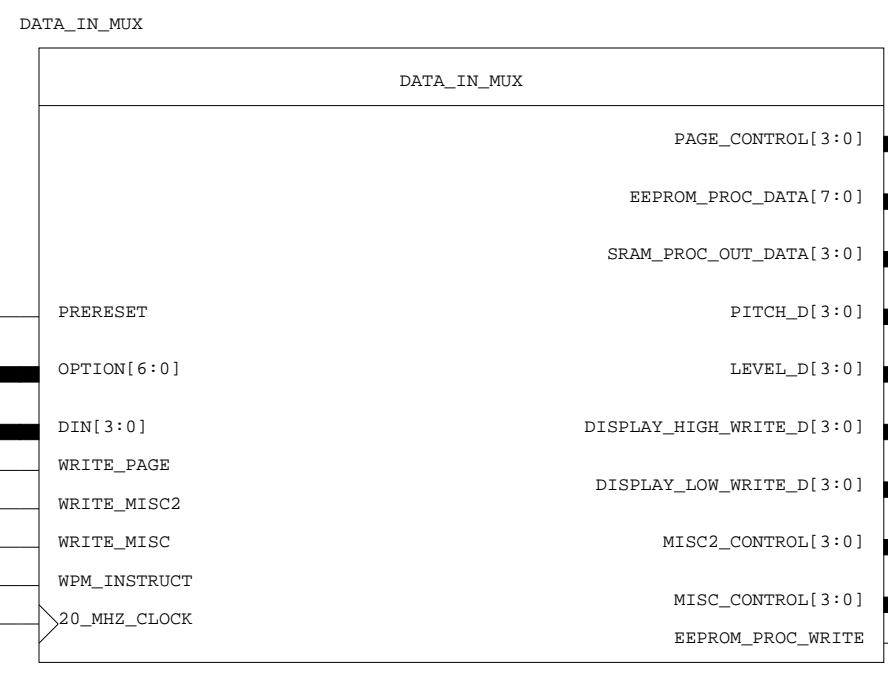
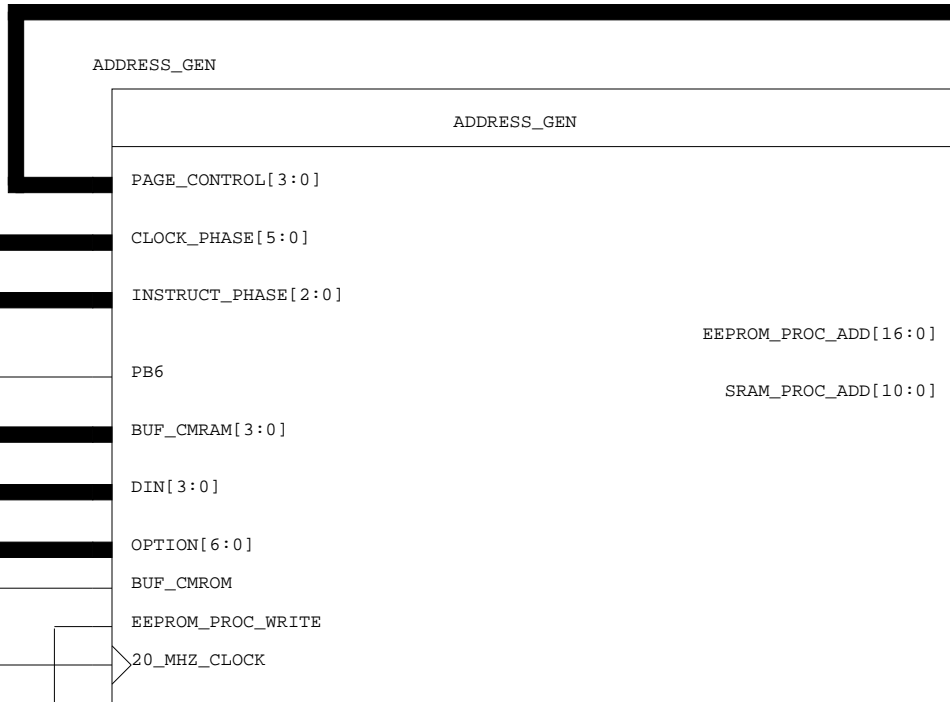
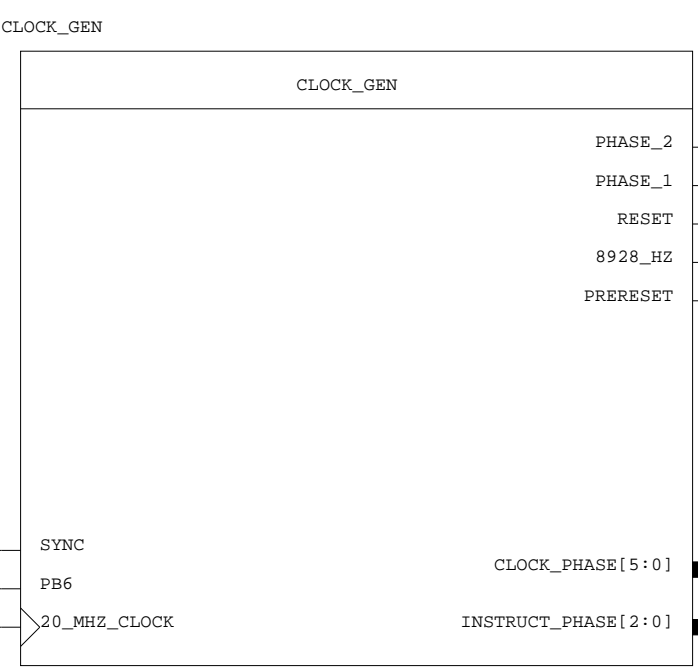
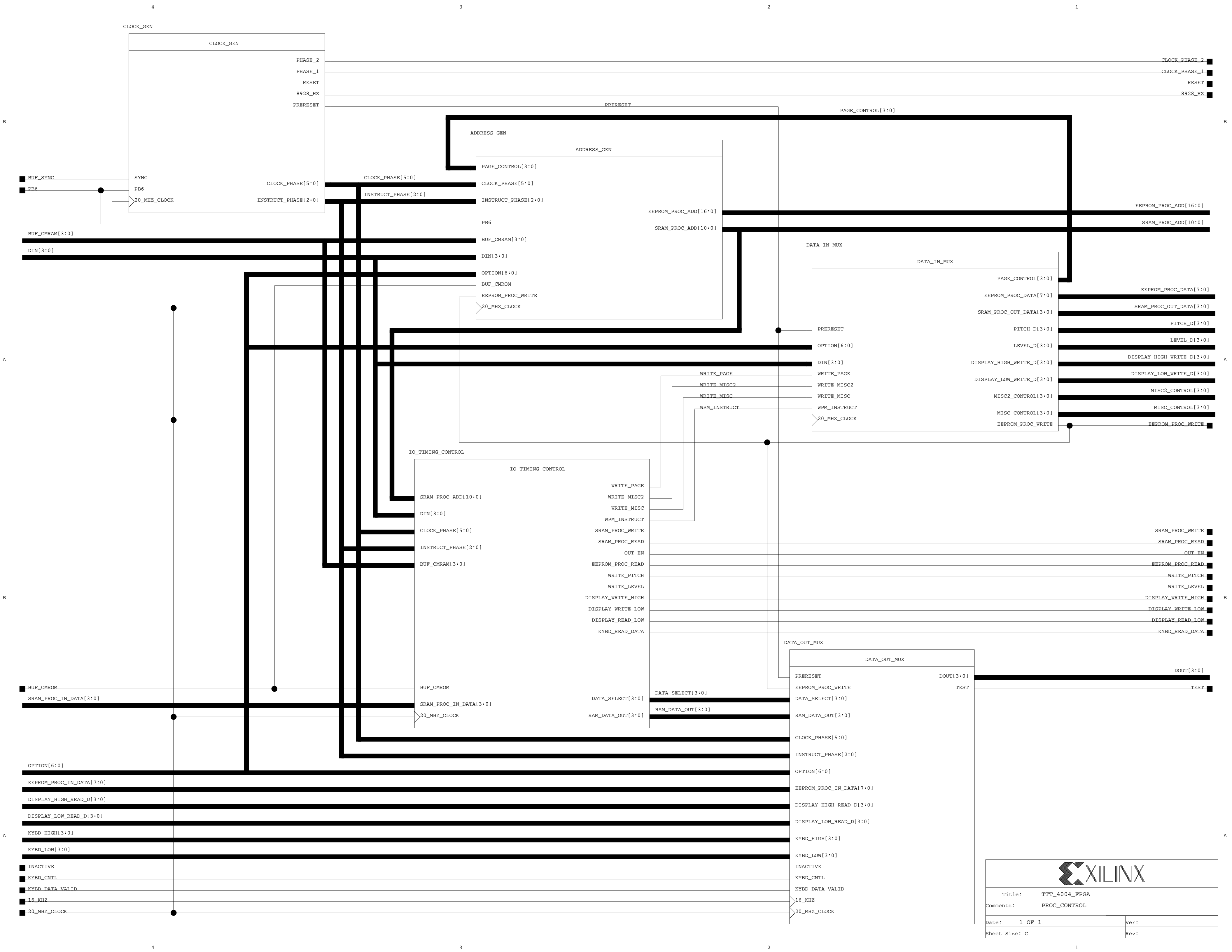
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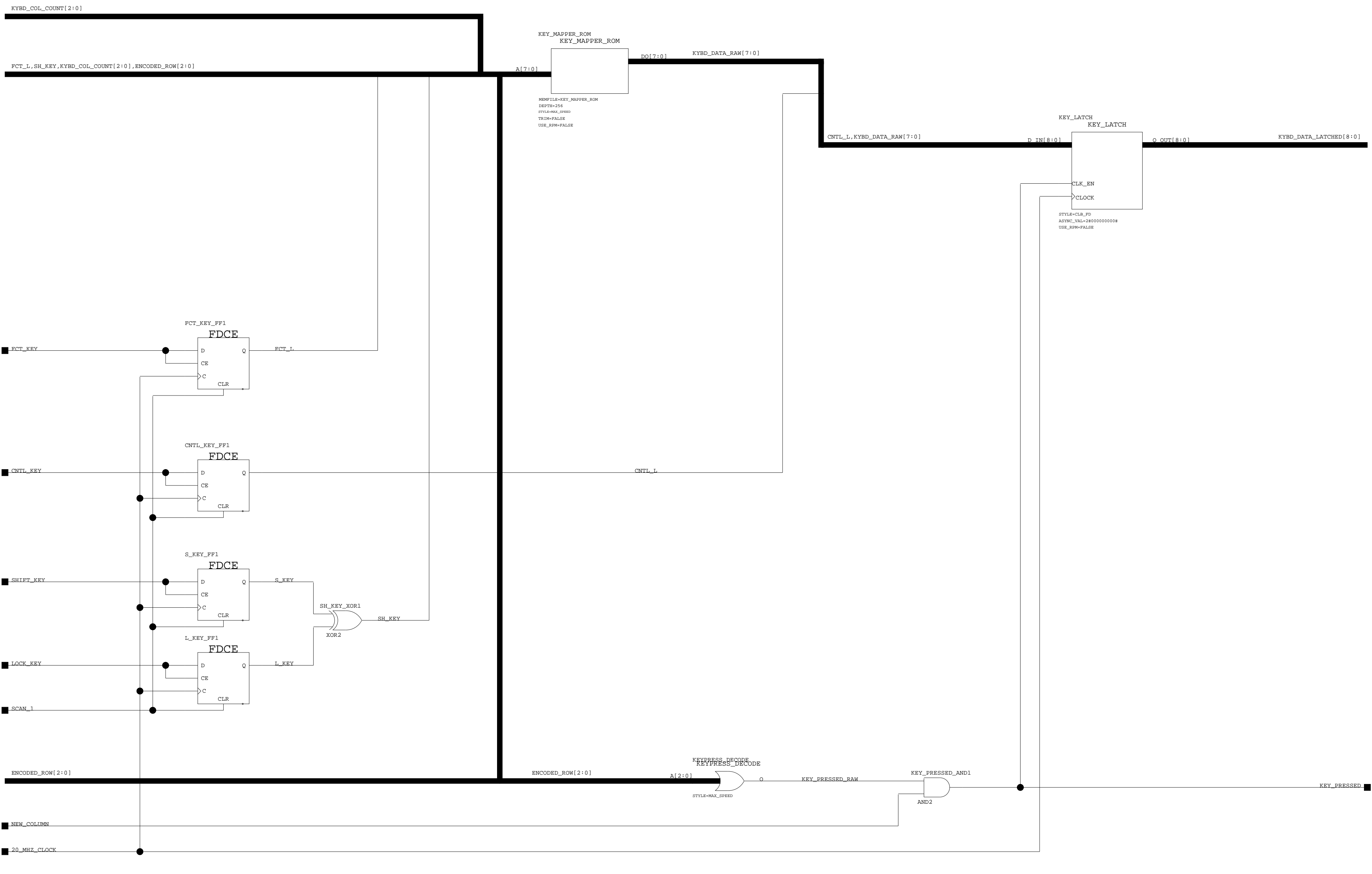
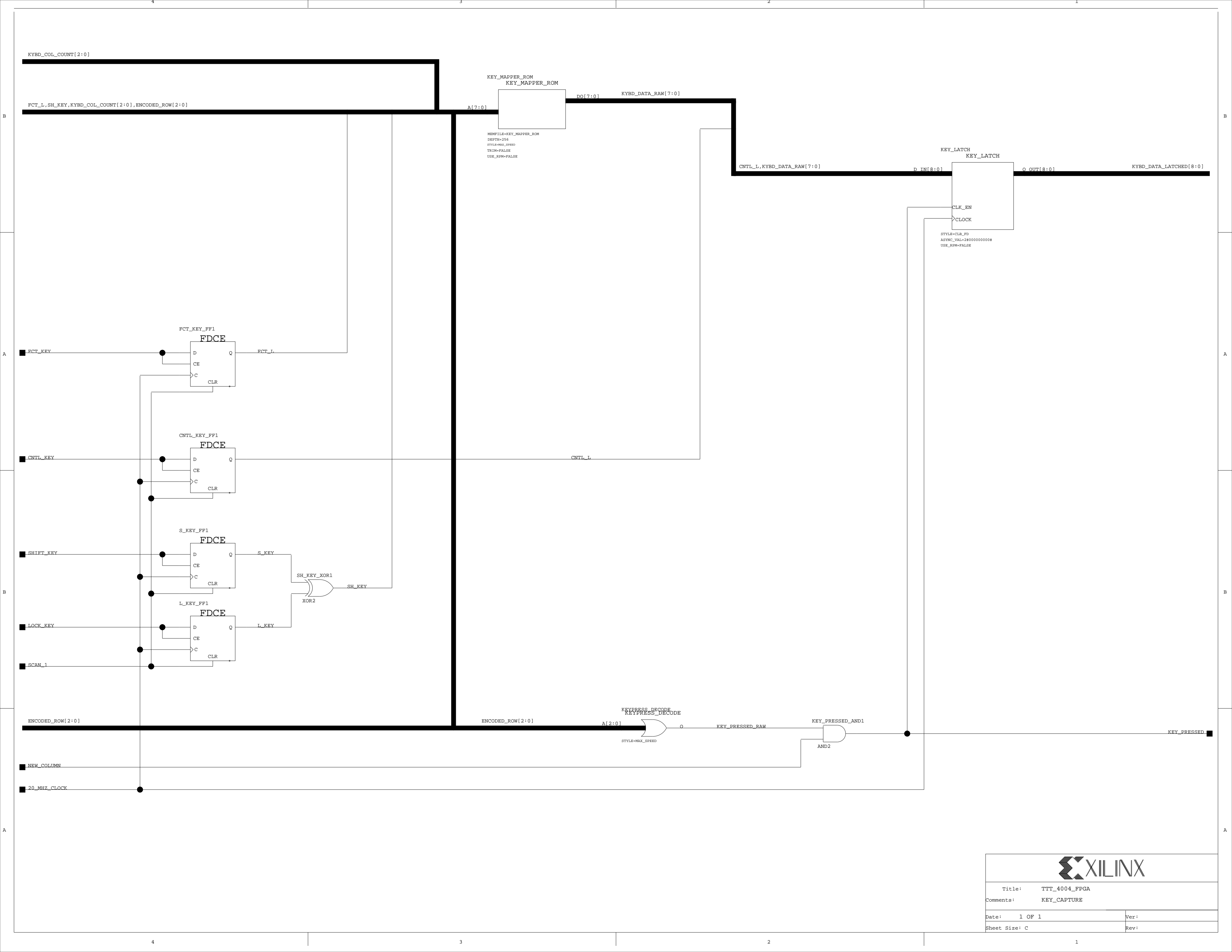
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Comments: SRAM_CONTROL	
Date: 1 OF 1	Ver:
Sheet Size: C	Rev:



- BUF\_SYNC
- PB6
- BUF\_CM RAM[3:0]
- DIN[3:0]
- BUF\_CMROM
- SRAM\_PROC\_IN\_DATA[3:0]
- OPTION[6:0]
- EEPROM\_PROC\_IN\_DATA[7:0]
- DISPLAY\_HIGH\_READ\_D[3:0]
- DISPLAY\_LOW\_READ\_D[3:0]
- KYBD\_HIGH[3:0]
- KYBD\_LOW[3:0]
- INACTIVE
- KYBD\_CNTL
- KYBD\_DATA\_VALID
- 16\_KHZ
- 20\_MHZ\_CLOCK

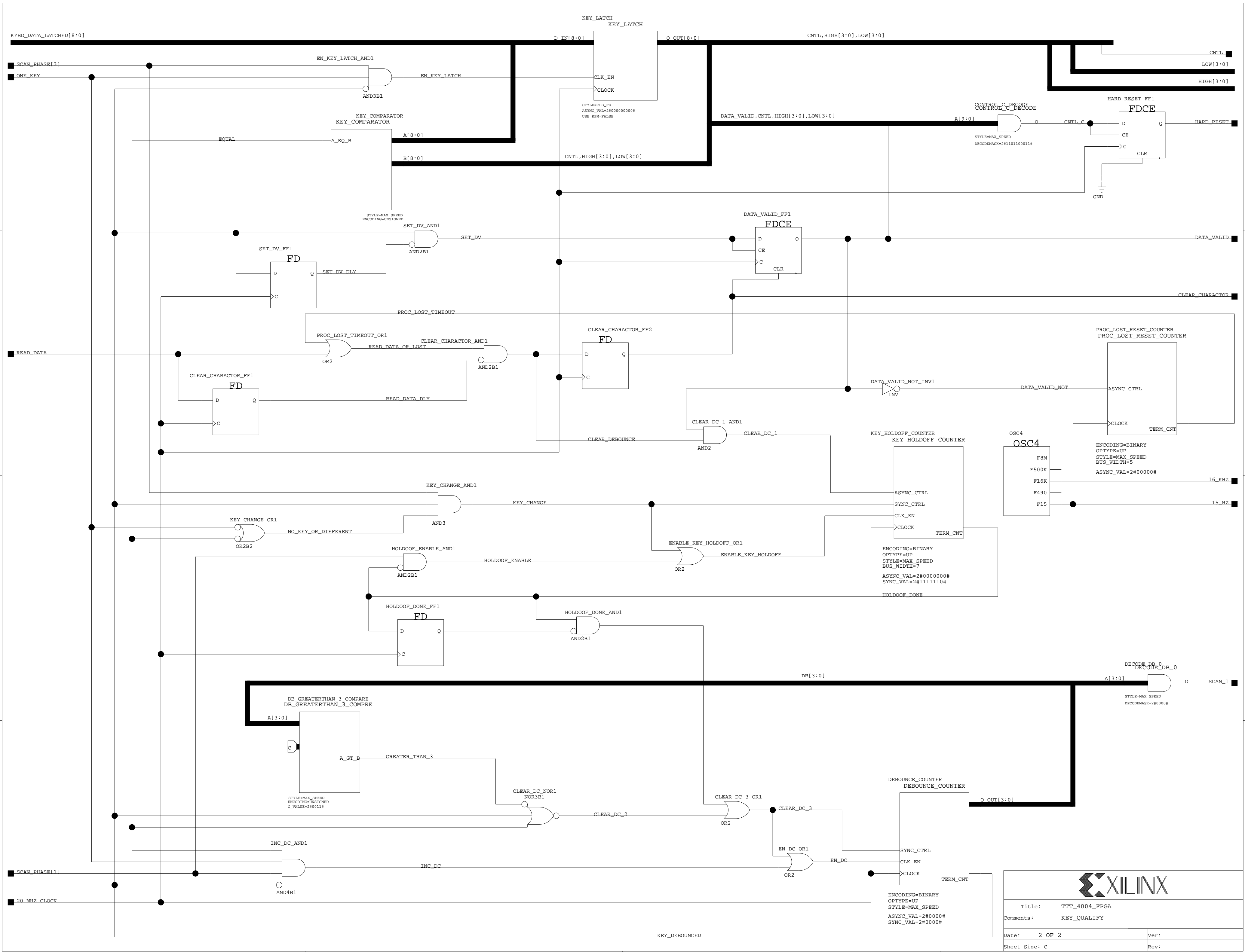
- CLOCK\_PHASE\_2
- CLOCK\_PHASE\_1
- RESET
- 8928\_HZ
- EEPROM\_PROC\_ADD[16:0]
- SRAM\_PROC\_ADD[10:0]
- EEPROM\_PROC\_DATA[7:0]
- SRAM\_PROC\_OUT\_DATA[3:0]
- PITCH\_D[3:0]
- LEVEL\_D[3:0]
- DISPLAY\_HIGH\_WRITE\_D[3:0]
- DISPLAY\_LOW\_WRITE\_D[3:0]
- MISC2\_CONTROL[3:0]
- MISC\_CONTROL[3:0]
- EEPROM\_PROC\_WRITE
- SRAM\_PROC\_WRITE
- SRAM\_PROC\_READ
- OUT\_EN
- EEPROM\_PROC\_READ
- WRITE\_PITCH
- WRITE\_LEVEL
- DISPLAY\_WRITE\_HIGH
- DISPLAY\_WRITE\_LOW
- DISPLAY\_READ\_LOW
- KYBD\_READ\_DATA
- DO UT[3:0]
- TEST





Title: TTT_4004_FPGA	
Comments: KEY_CAPTURE	
Date: 1 OF 1	Ver:
Sheet Size: C	Rev:





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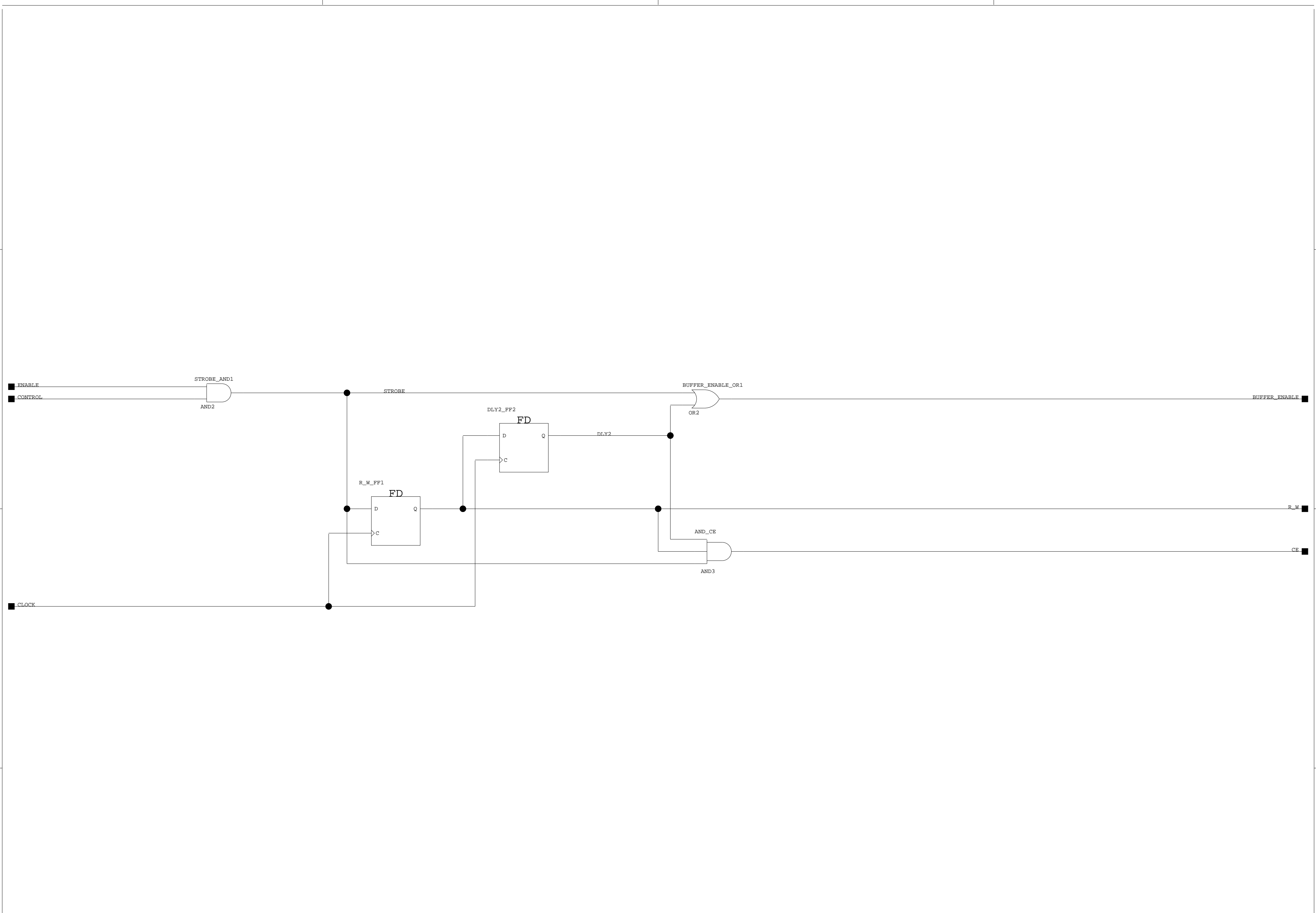
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Date: 1 OF 1	Ver:
Sheet Size: C	Rev:

B

B

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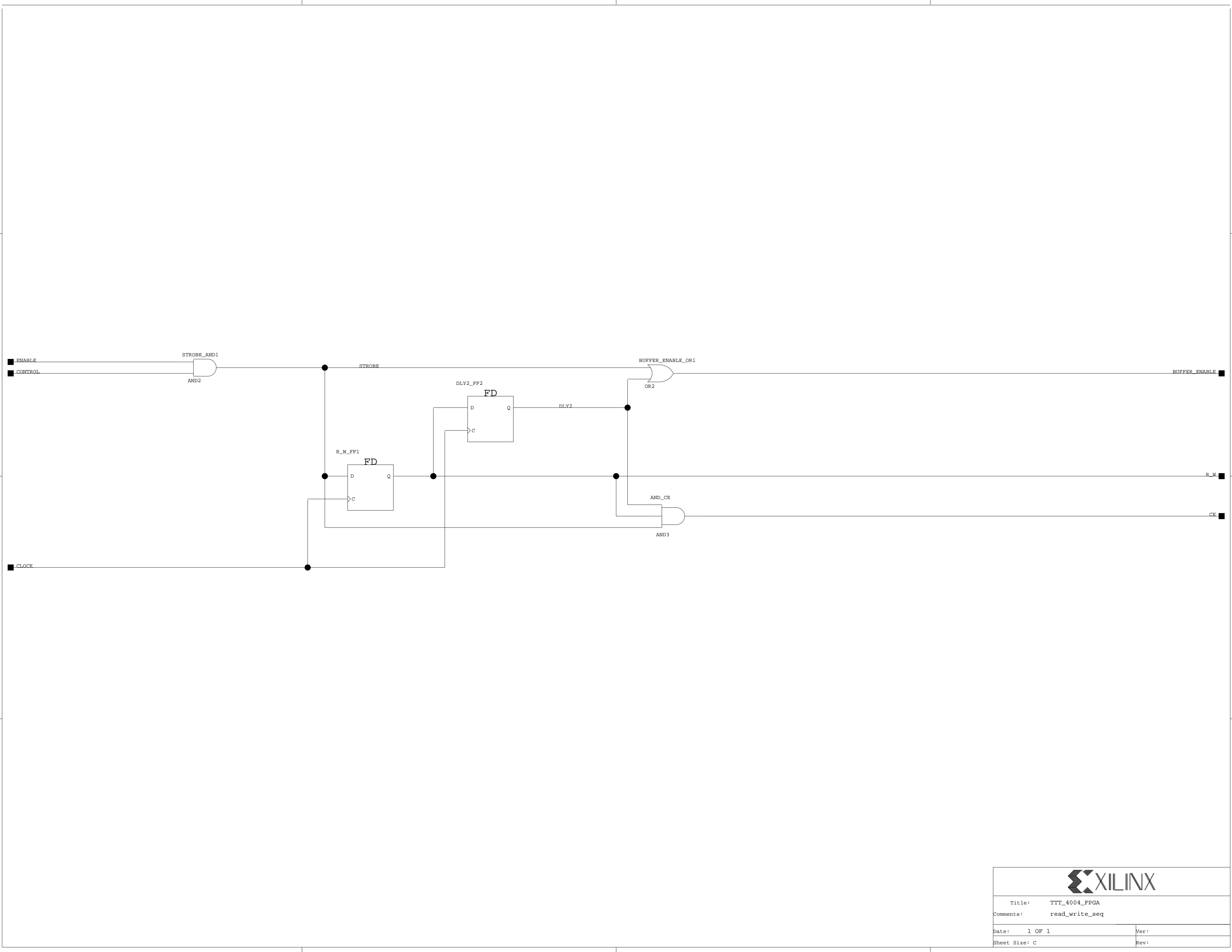
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Title: TTI_4004_FPGA	
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Sheet Size: C	Rev:

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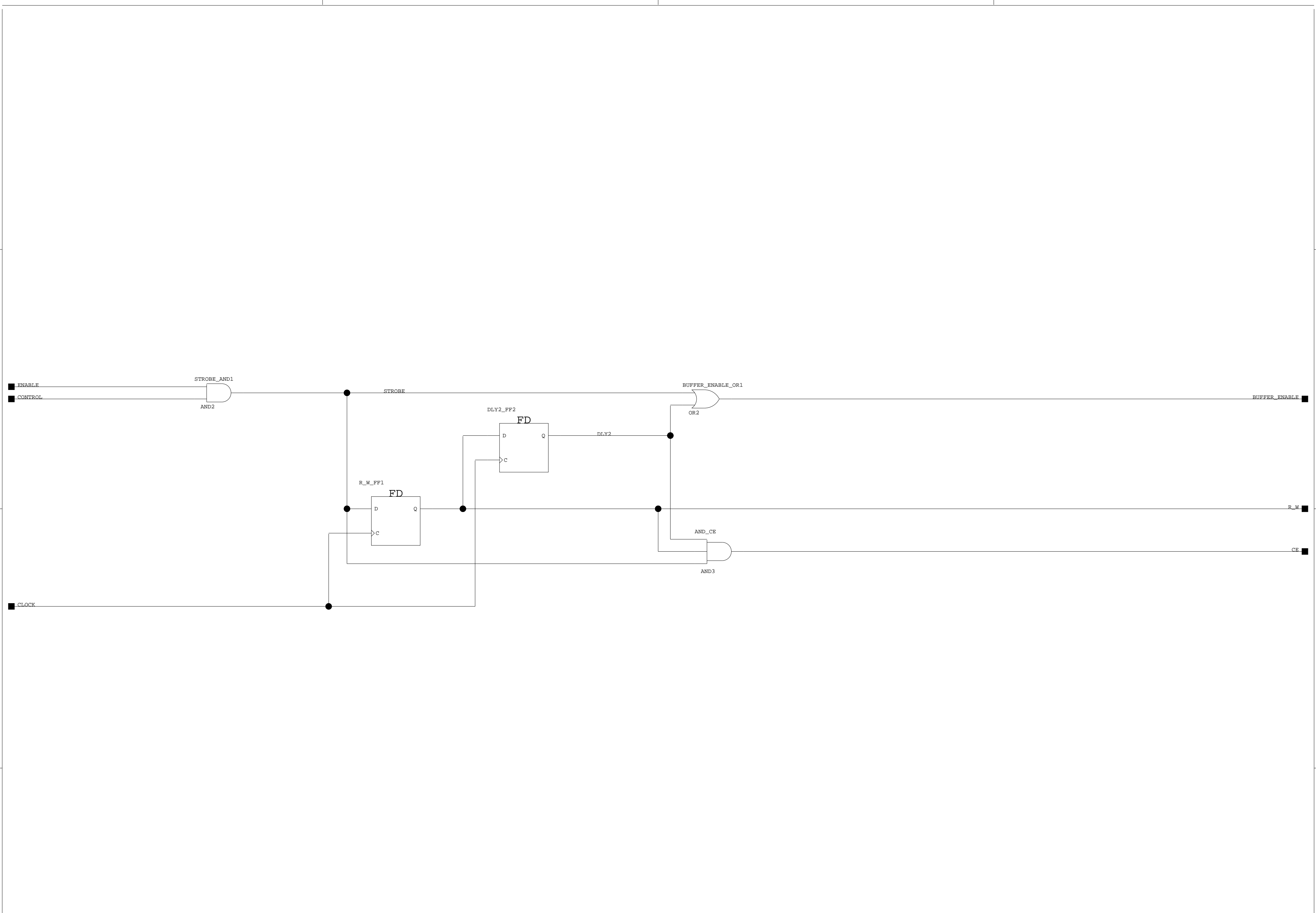
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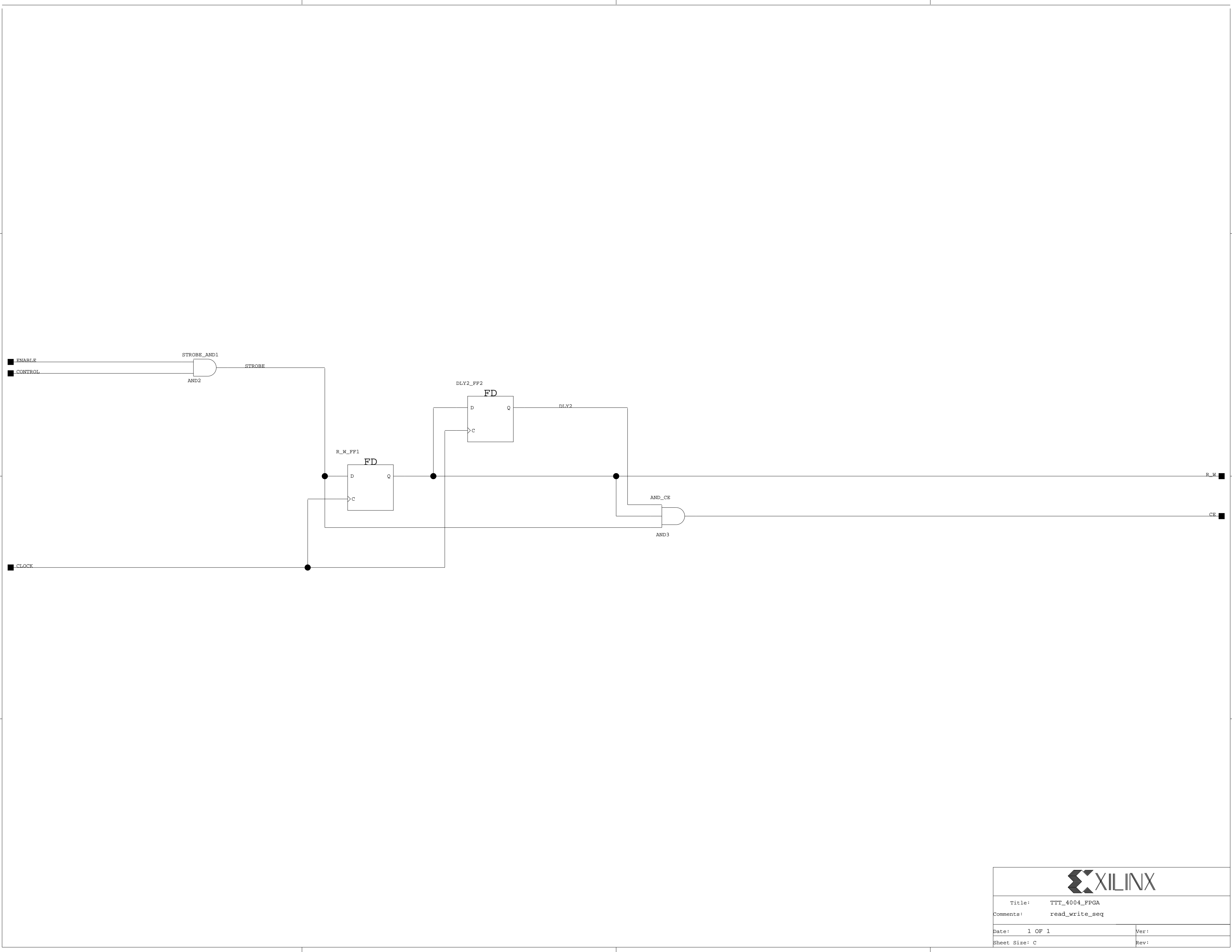
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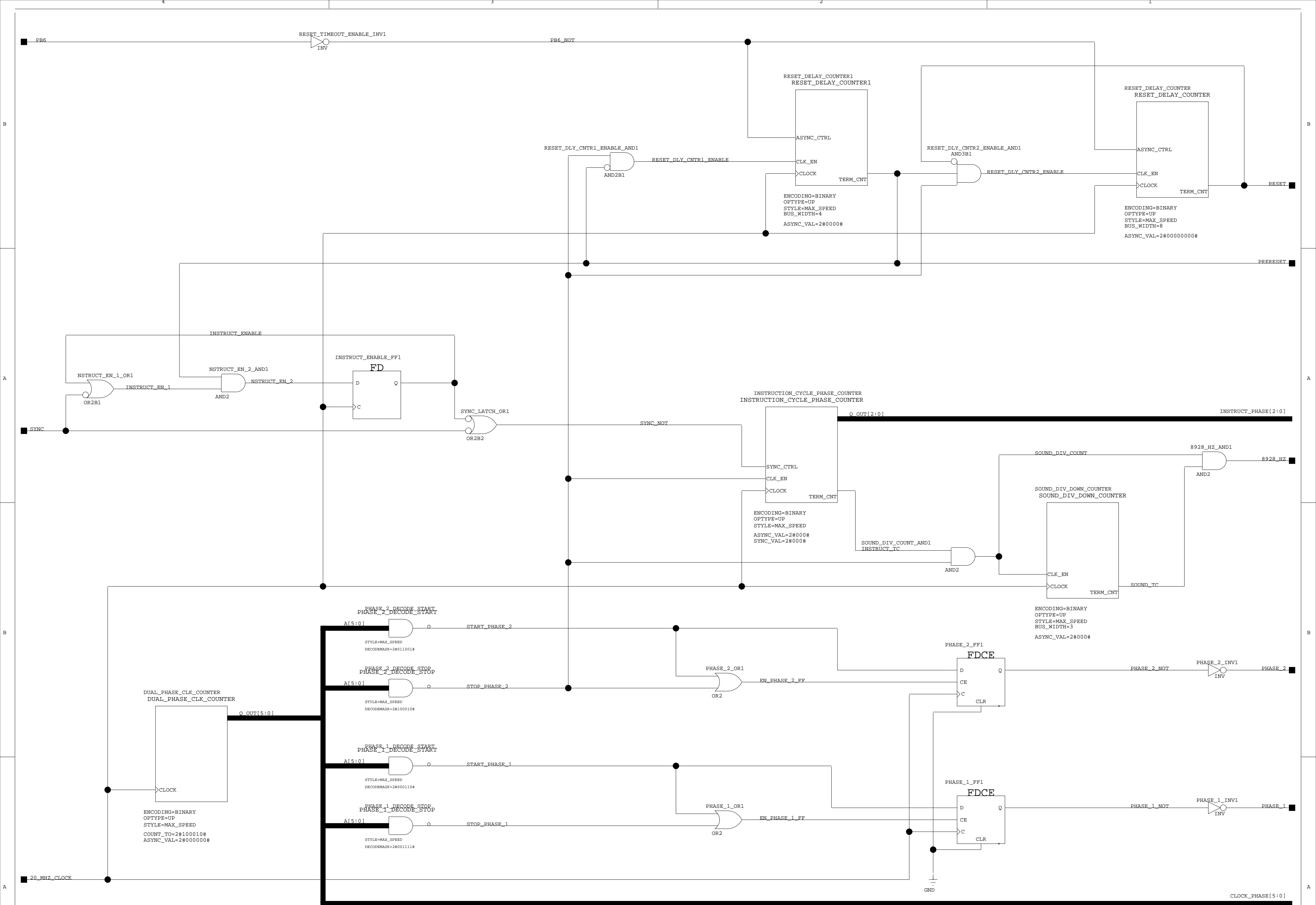
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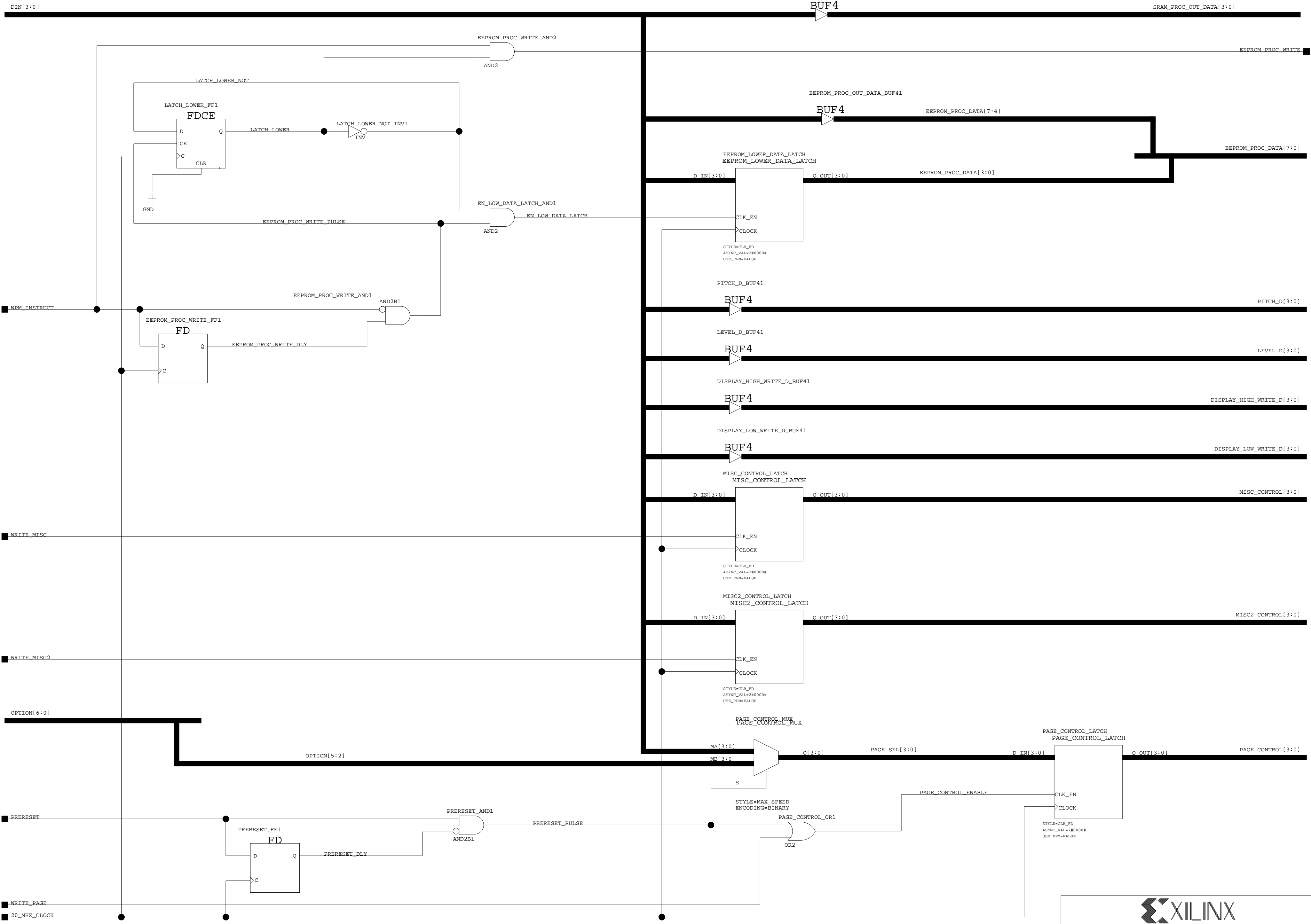
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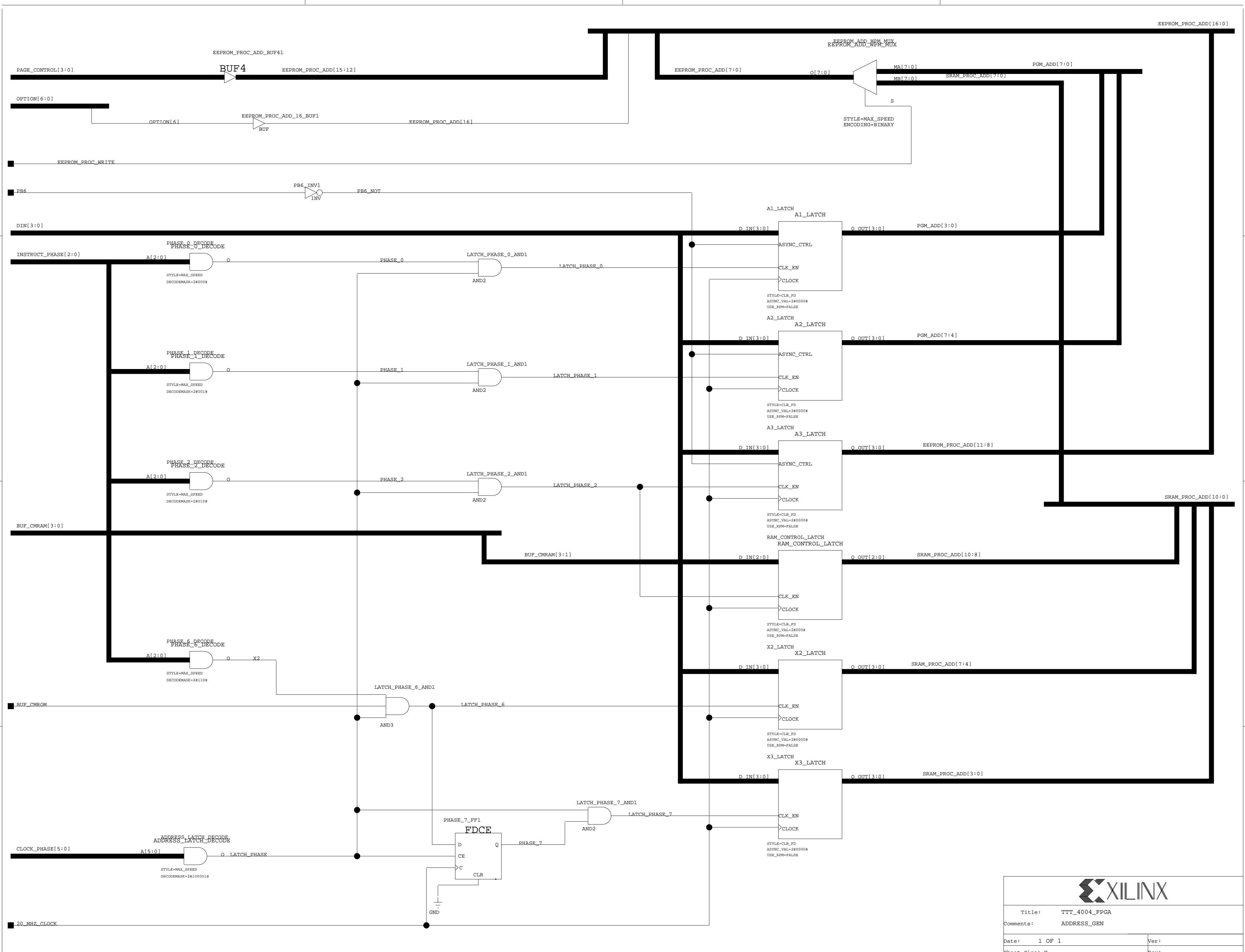
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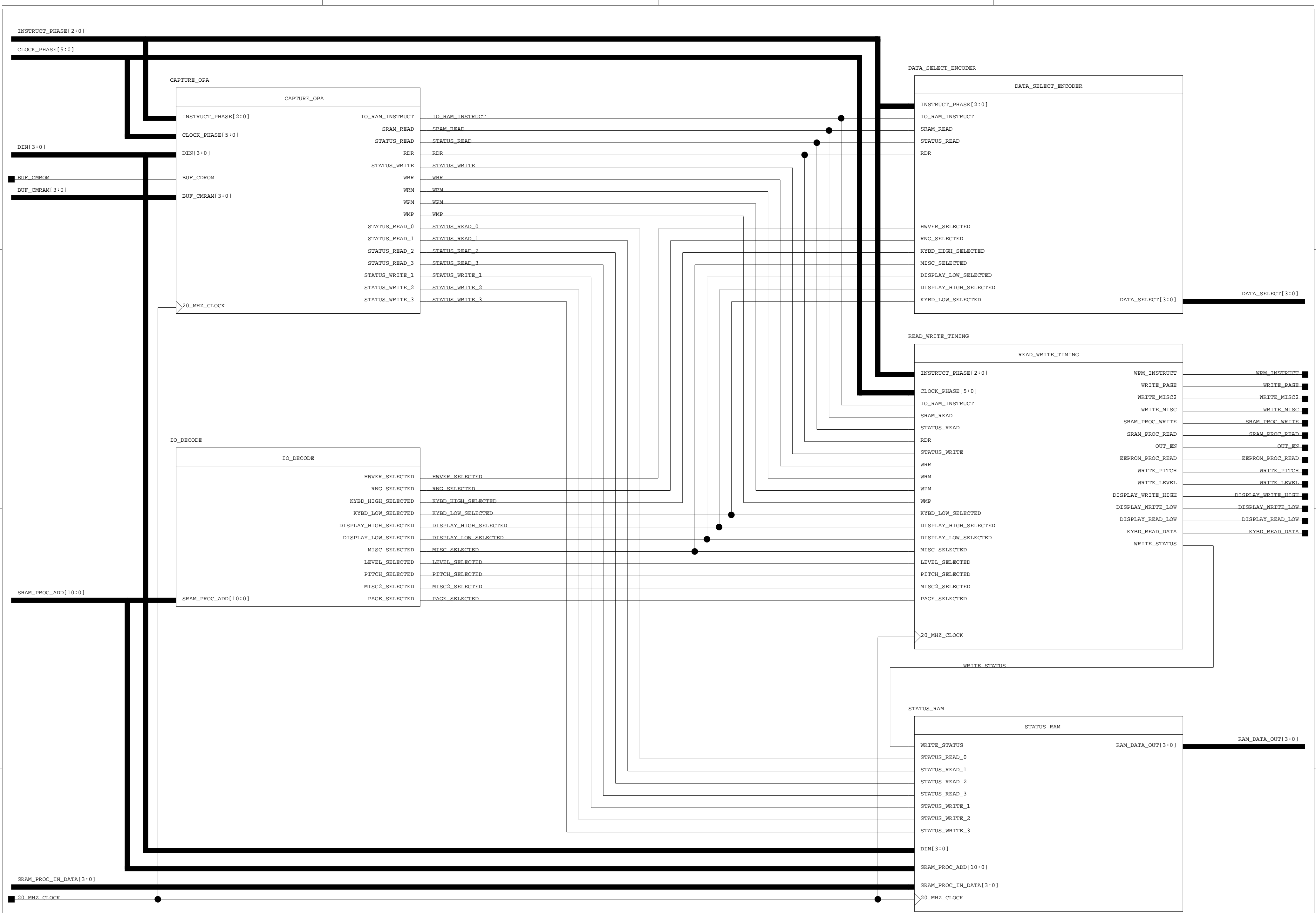
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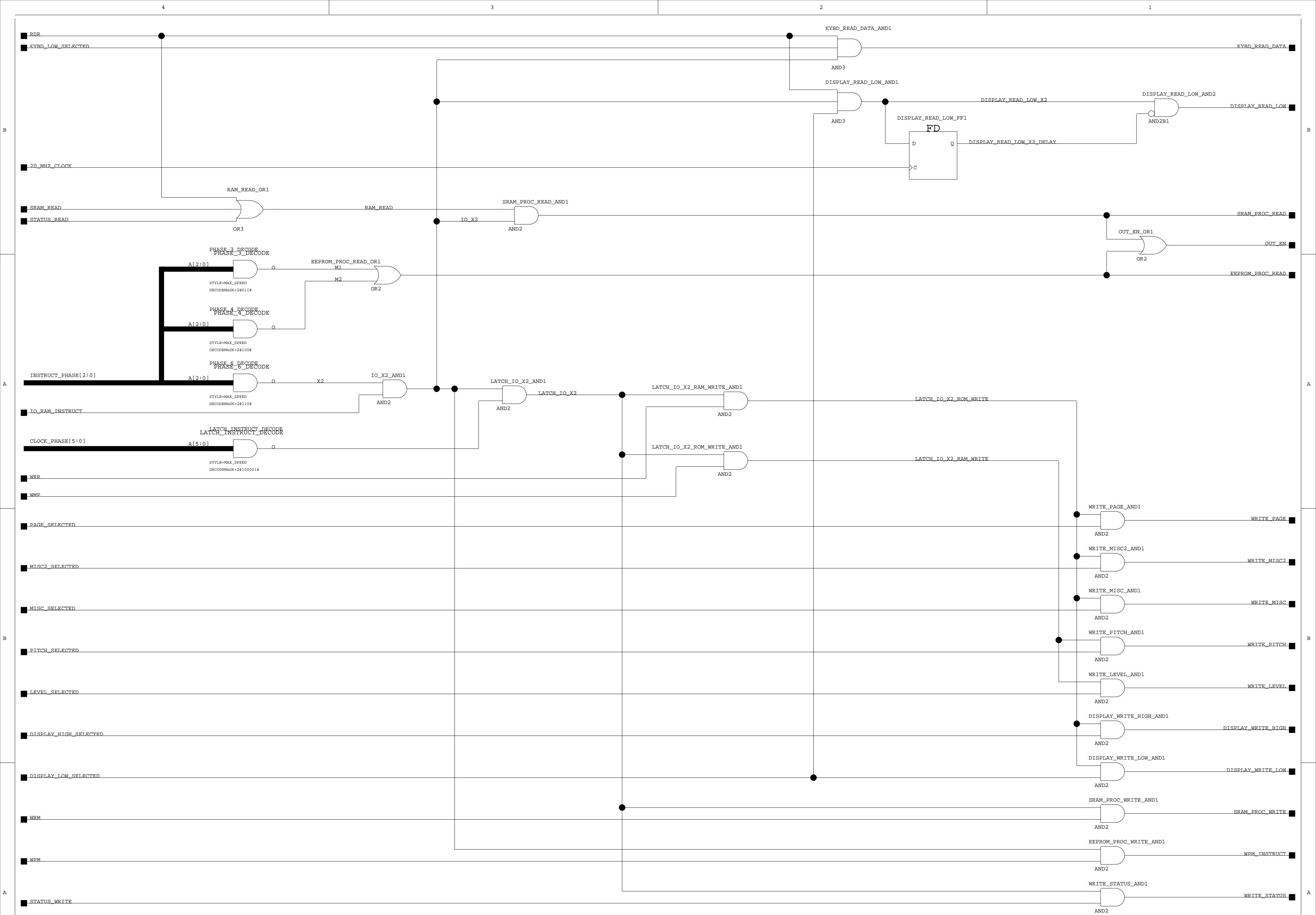


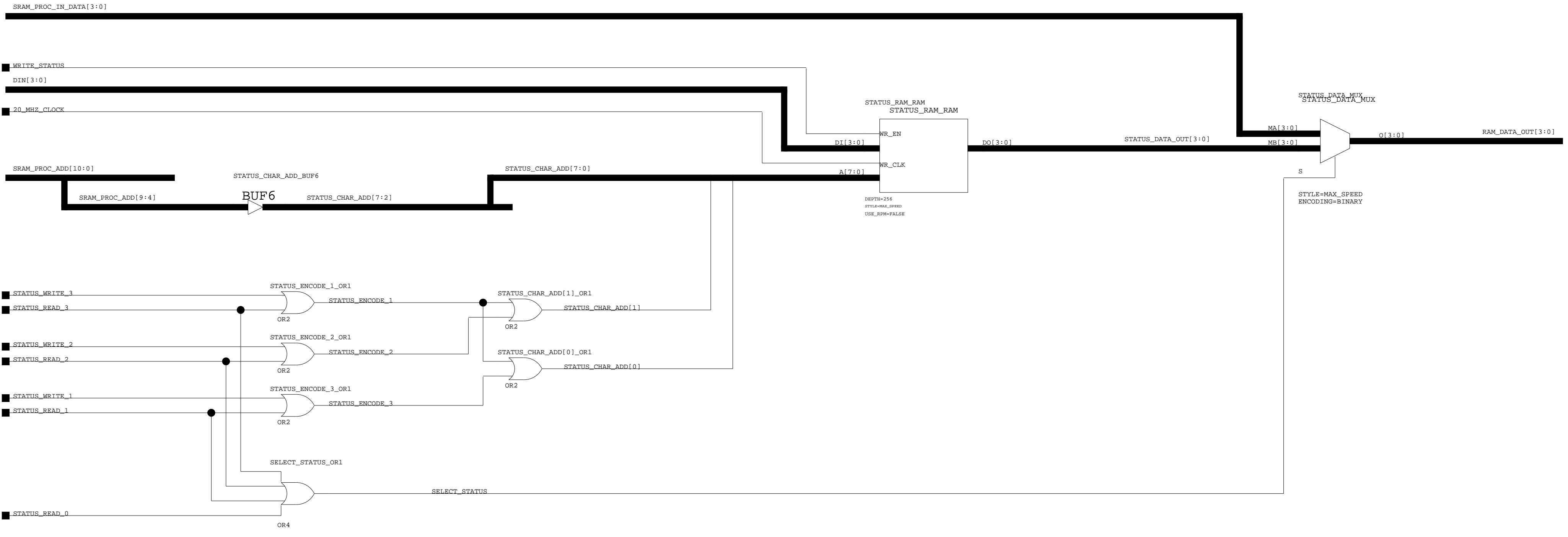




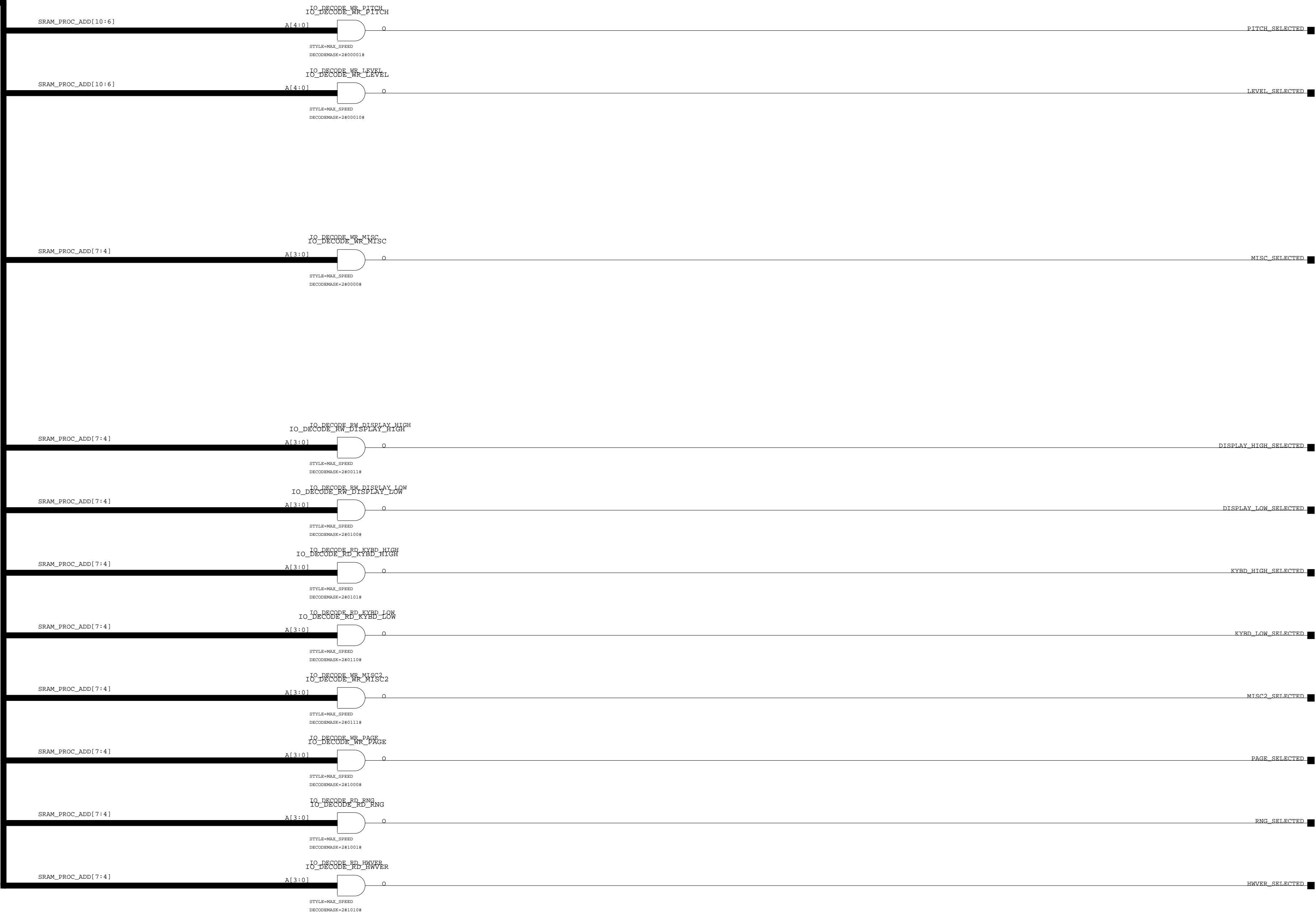
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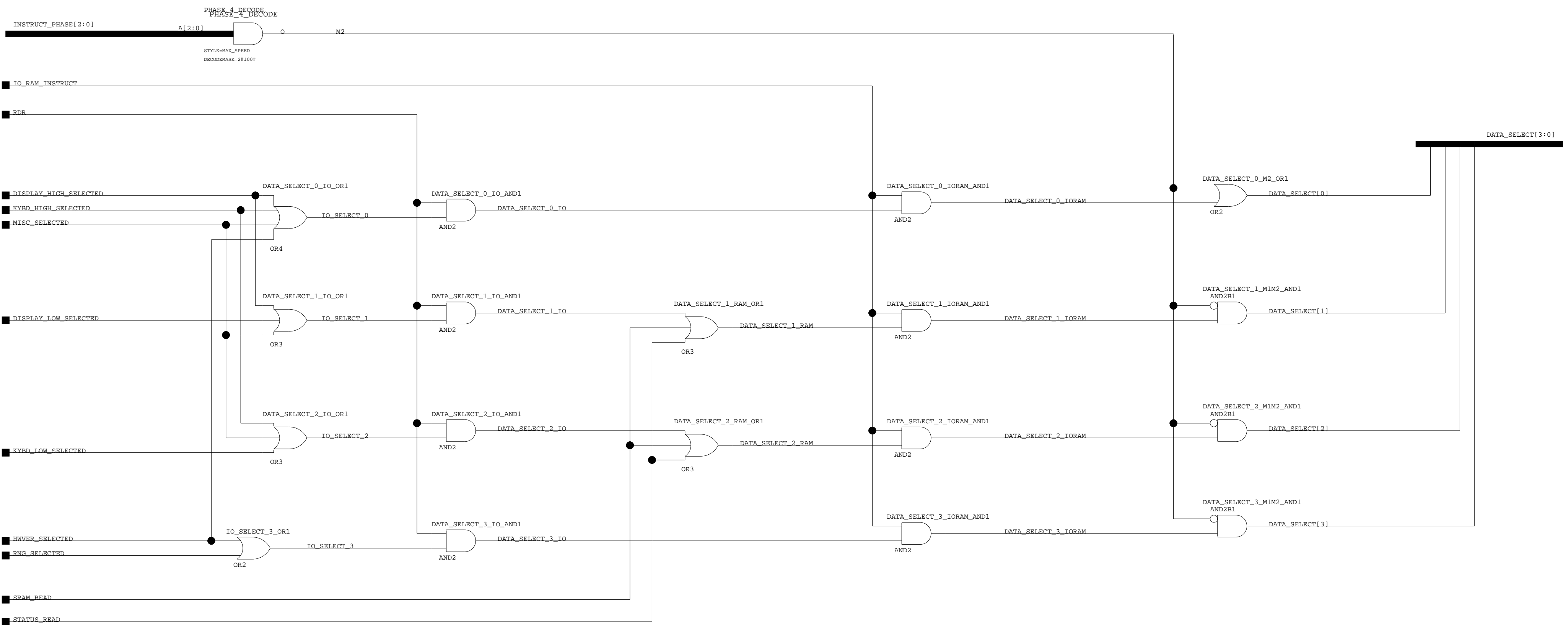


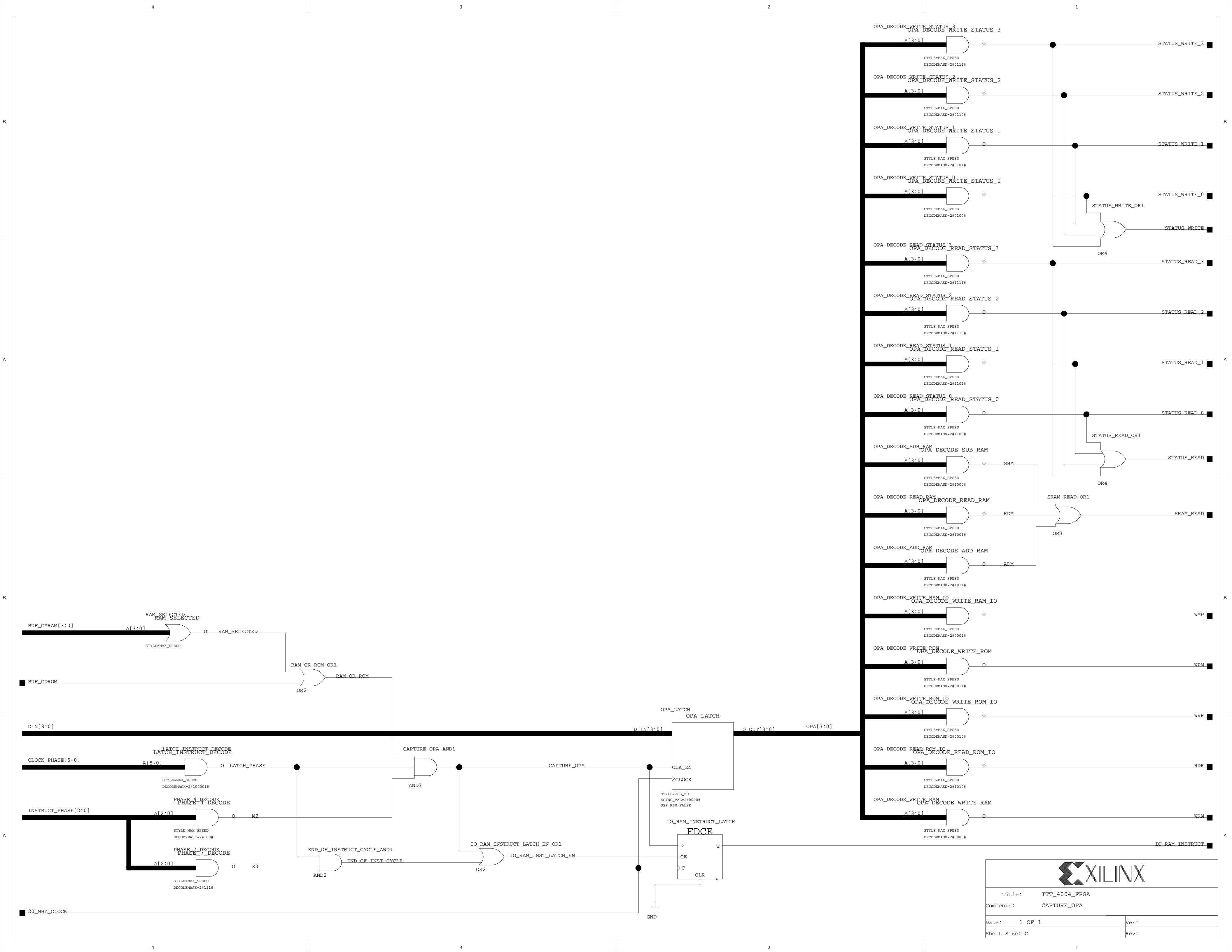


SRAM\_PROC\_ADD[10:0]



Title: TTI_4004_FPGA	
Comments: IO_DECODE	
Date: 1 OF 1	Ver:
Sheet Size: C	Rev:





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Comments: CAPTURE_OPA	
Date: 1 OF 1	Ver:
Sheet Size: C	Rev: