

Hacking the Si4734

Hardware Handbook for Shortwave

VERSION 2 ©2010

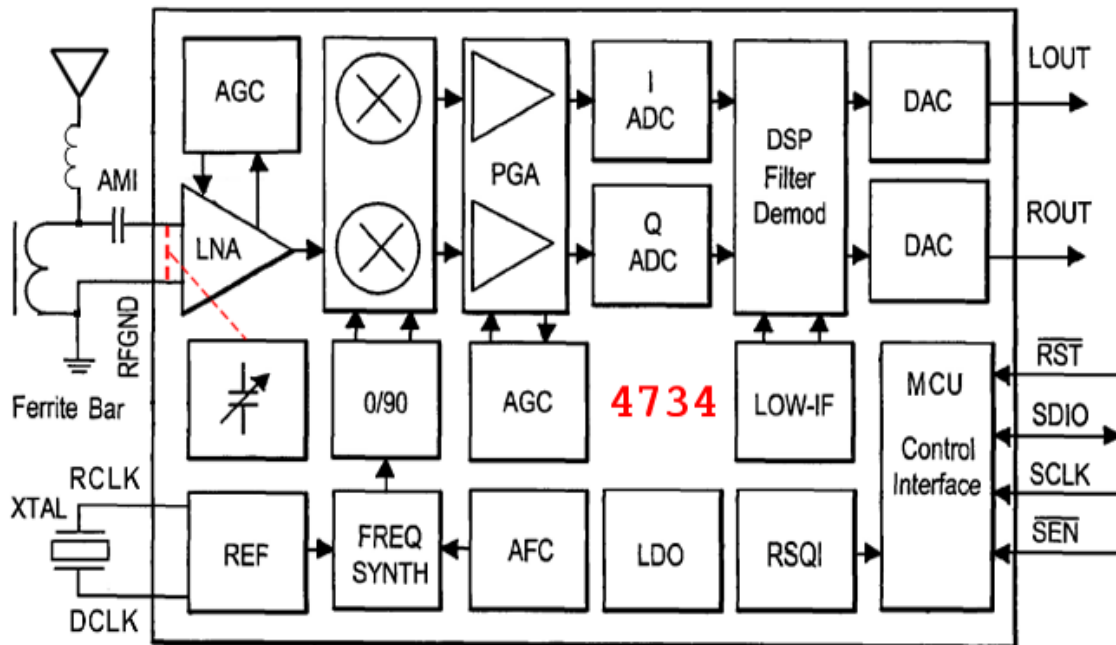


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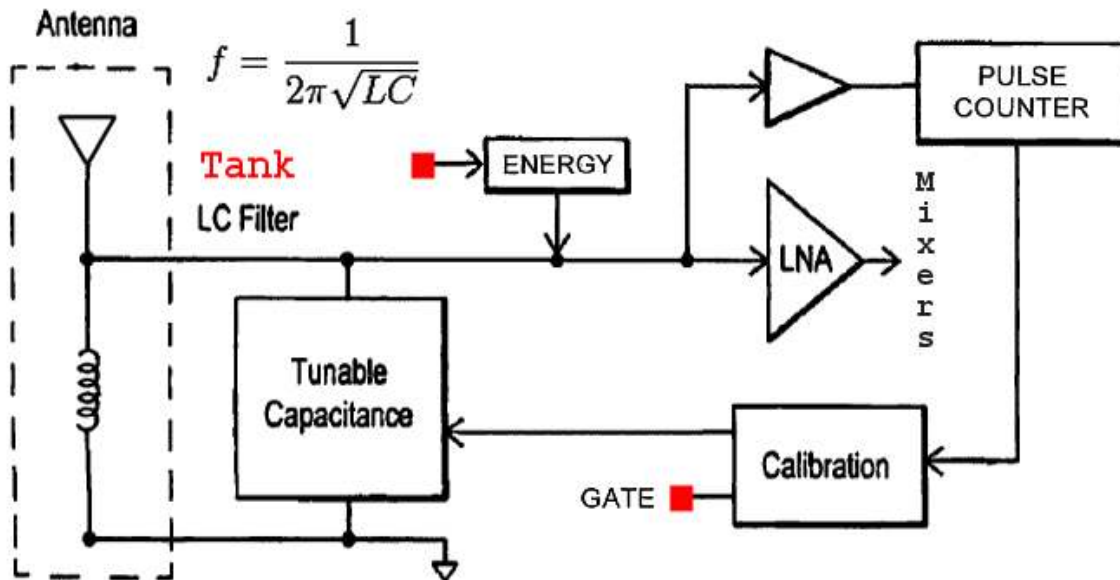
| Si4734 Frequency Coverage | | |
|---------------------------|--------------|------------------------------------|
| LW | 153- 279 kHz | talk, Europe, Africa 2800 μ H |
| MW | 520-1710 kHz | talk, 180-450 μ H ¹ |
| SW | 2.3- 23 MHz | global, China, India, Brazil |
| FM | 64- 76 MHz | college, emergency, TV |
| FM | 76- 108 MHz | global |

¹Mating a 15 μ H air loop to a 1:5 ratio inductor yields 375 μ H.

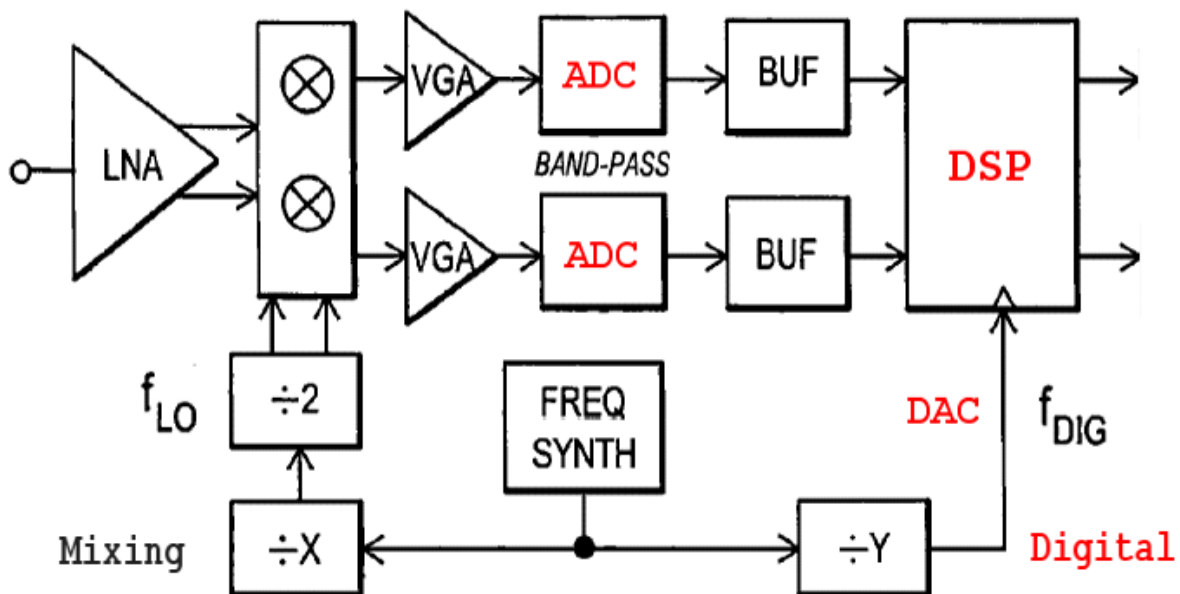
Silicon Labs is revolutionizing radio with their Si4734: a CMOS AM/FM/SW/LW low-IF DSP receiver chip. This IC is part of a new era wherein portables will no longer need ceramic IF filters. Radio design will instead focus on the antenna circuit, audio amplification (ex. Sony CXA1622M), user interface, and MCU control. These radios will require little or no manual (factory) alignment.



Tuned RF energy (see below) enters a low noise amplifier (LNA) whose gain is under MCU control. The automatic gain control (AGC) can also adjust the programmable gain amplifier (PGA) that follows each mixer. The I/Q (Inphase/Quadrature) lines are digitized using low- or band-pass high-resolution analog to digital converters (ADC). A digital low-IF (intermediate frequency) signal is presented to a digital signal processor (DSP) for bandwidth limiting and demodulation. This digital section is 24-bit and capable of sampling at 48-kHz. A digital to analog converter (DAC) creates a high impedance (10k-ohm) audio signal (THD 0.1%) to be boosted by an external audio amplifier. The Si4734 also contains a low dropout voltage regulator (LDO) [two 1.5 Volt batteries can supply both VDD and VIO], an automatic frequency control (AFC), a radio signal quality interrupt (RSQI) line, and a separate FM section [includes FM input line (PIN 2; FMI), FM LNA, and FM I/Q mixers].



One unique feature of the Si4734 is its ability to automatically tune AM antennas. During AM operation the antenna's external inductor forms a tank with the chip's internal capacitor. The (calculated) tuning range of the internal capacitance is from 7.095 to 590.585 pF. The low noise amplifier input is of high impedance. The capacitor value can also be manually set during tuning. Multiple weighted parallel MOS capacitors, each with a transistor switch, are under 13-bit digital control. The chip enters a calibration mode when a new station is tuned. Under MCU control (red square above), energy is added to the tank by forcing current in its inductor (DC is converted to AC). This energy dissipates via damped oscillations (ringing) at the tank's resonant frequency. A pulse counter (fed by a high input impedance amplifier) determines the frequency of the ringing. The MCU iteratively adjusts the IC's tunable capacitance until the resonant frequency of the tank equals the desired (sought or tuned) frequency. I wish to thank [Scott Willingham](#) of Silicon Labs.

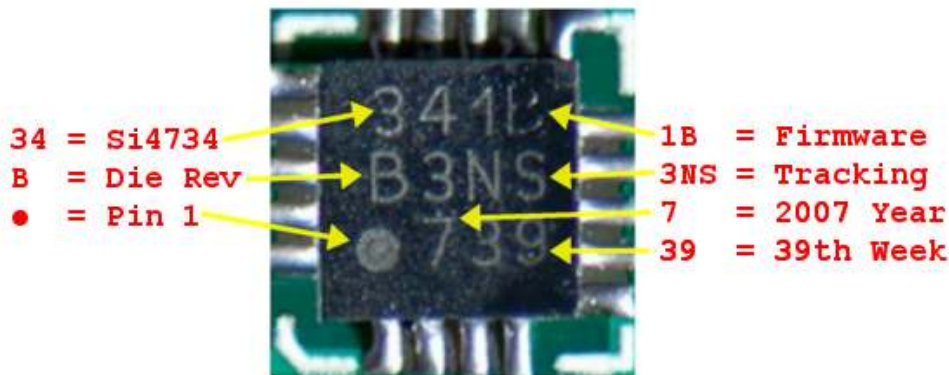


The Si4734 also contains a ratiometric clock, meaning a single oscillator is divided down for use by both the local oscillator (divide by 2 providing I/Q signals) and the digital circuitry. In doing this, digital harmonics fall on the frequency of the oscillation signal. This feature permitted Silicon Labs to pack a DSP, ADC, DAC, MCU, and other clocked digital components on a chip that contains LO generation and RF mixers. The chip is capable of low and high-side LO injection. The design supports a programmable IF. The chip is capable of correcting for frequency inaccuracies. The Si4734 is firmware upgradeable and up to **15,856** bytes can be written as a software patch.



COB

The Si4734 contains advanced [wireless communications technology](#). It has incorporated [ESD](#) (electrostatic discharge) protection (two input protection diodes) for its low noise amplifier (LNA). Its LNA has a digitally controlled attenuation network (variable bias resistance). The chip contains a digital automatic gain control ([AGC](#)). Peak detection circuits are located after the LNA and each VGA. A digital processor (apart from the main DSP) uses the detectors (set to high and low thresholds) to incrementally adjust the gain. If the [RSSI](#) (Received Signal Strength Indicator) does not track the change in gain of the LNA (1 dB RSSI per dB gain) then a flag is set indicating possible [intermodulation](#) distortion. The MCU can correct the situation by reducing amplifier gain. The gain is adjusted from the antenna (LNA) inward. The ADC sets an overload line ([O/L](#)) when a repetition of output occurs over several clock cycles (gain being high, SNR low, noise floor high). The Si4734 has an unconditionally stable ADC based on a delta-sigma modulator ([DSM](#)). Its ADC can maintain stability regardless of the amplitude or frequency of the incoming signal. DSM was used to permit high resolution conversion by means of a low-cost [CMOS](#) manufacturing process.



The [20-pin](#) Si4734 is [3 mm](#) square and housed in a [QFN](#) package. Manufacturers also use chips that are mounted on an 18-pin board or [COB](#) (chip on board) assembly. Each chip has [YAG](#) laser surface markings. The "34" denotes a Si4734 and is followed by the firmware version. Next is the die revision, here "B", followed by a three digit tracking code. The circle denotes PIN 1 and is followed by year "7" (meaning 2007) and by 2 week digit codes "39" (meaning the 39th week).

The sensitivity specification for the Si4734 on AM is given as: [25 \$\mu\$ V](#) for [26 dB](#) (S+N)/N. It was calculated that the receiver chip, at [3 dB](#) (S+N)/N, has a sensitivity of [1.77 \$\mu\$ V](#) or about [S4](#). An [S2](#) (0.4 μ V) signal can be heard with [+12.9 dB](#) gain: this is achievable via toroid turns ratios.

REFERENCE

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