



DESCRIPTION

PT2399 is an echo audio processor IC utilizing CMOS Technology which is equipped with ADC and DAC, high sampling frequency and an internal memory of 44K. Digital processing is used to generate the delay time, it also features an internal VCO circuit in the system clock, thereby, making the frequency easily adjustable. PT2399 boasts of very low distortion (THD<0.5%) and very low noise (No<-90dBV), thus producing high quality audio output. The pin assignments and application circuit are optimized for easy PCB layout and cost saving advantage.

FEATURES

- CMOS Technology
- Least External Components
- Auto Reset Function
- Low Noise, No<-90dBV Typical
- Low Distortion, THD<0.5% Typical
- External Adjustable VCO
- Available in 16 pins, DIP or SO package

APPLICATIONS

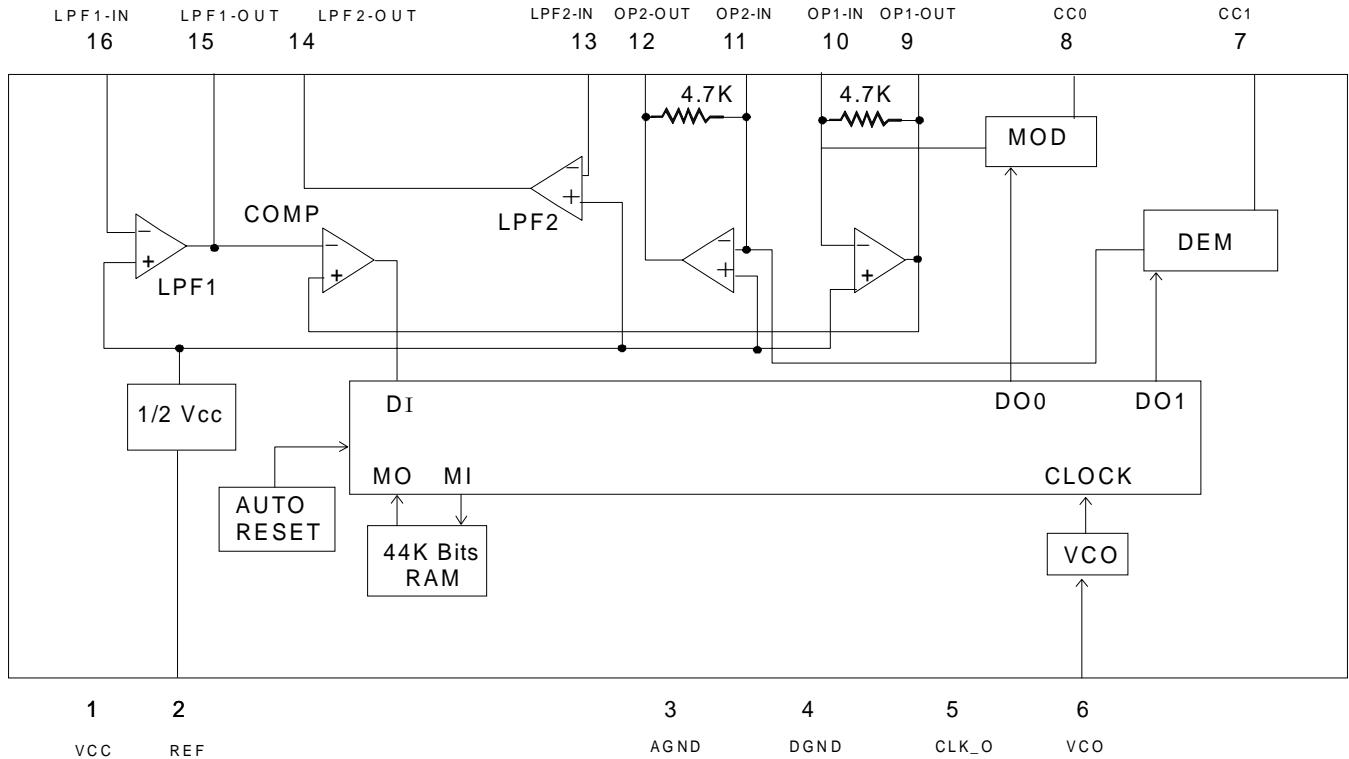
- Video Tape Recorder
- Video Compact Disk
- Television
- CD Player
- Car Stereo
- KARAOKE Mixer
- Electronic Musical Instrument
- Audio Equipment with Echo Processor



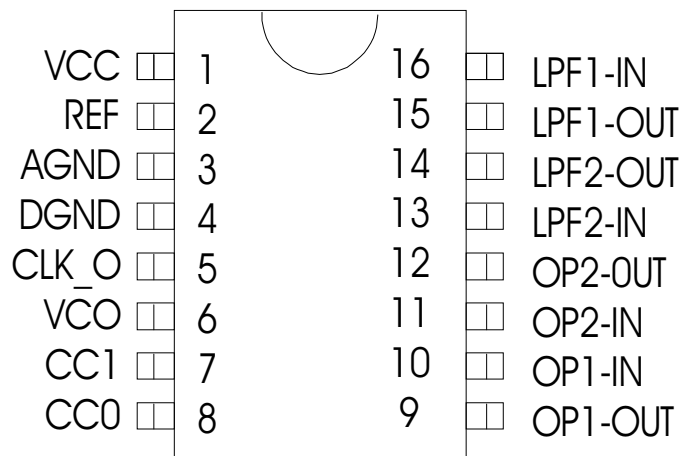
Echo Processor IC

PT2399

BLOCK DIAGRAM



PIN CONFIGURATION



PT2399



PIN DESCRIPTION

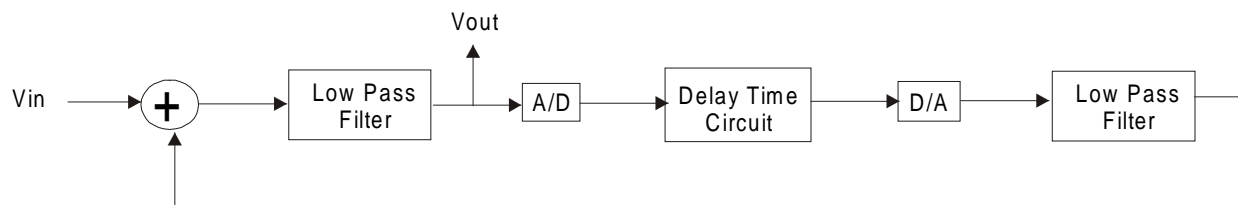
Pin Name	I/O	Description	Pin No.
VCC	-	Analog Supply Voltage Input	1
REF	-	Analog Reference Voltage (=1/2Vcc)	2
AGND	-	Analog Ground	3
DGND	-	Digital Ground	4
CLK_O	O	System Clock Output Pin	5
VCO	I	Frequency Adjustment Pin	6
CC1	-	Current Control 1	7
CC0	-	Current Control 0	8
OP1-OUT	O	OP Amplifier 1 Output This pin can be used as Modulated Integrator by connecting Capacitor.	9
OP1-IN	I	OP Amplifier 1 Input This pin can be used as Demodulated Integrator by connecting Capacitor.	10
OP2-IN	I	OP Amplifier 2 Input This pin can be used as Demodulated Integrator by connecting Capacitor.	11
OP2-OUT	O	OP Amplifier 2 Output This pin can be used as a Modulated Integrator by connecting Capacitor	12
LPF2-IN	I	Low Pass Filter 2 Input Pin	13
LPF2-OUT	O	Low Pass Filter 2 Output Pin	14
LPF1-OUT	O	Low Pass Filter 1 Output Pin	15
LPF1-IN	I	Low Pass Filter 1 Input Pin	16



FUNCTIONAL DESCRIPTION

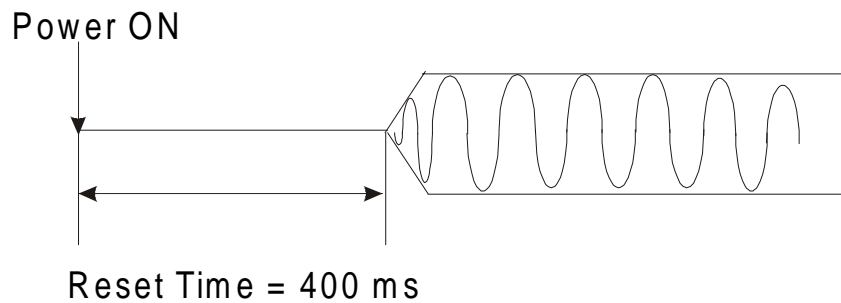
Echo Mode

Please refer to the diagram below:



Auto Reset Function

The waveform of the signal during Power On is given below:





ABSOLUTE MAXIMUM RATINGS

(Ta=25°C, unless otherwise specified)

Symbol	Description	Limits	Unit
Vcc	Supply Voltage	6.5	V
Icc	Supply Current	100	mA
Pd	Power Dissipation	1.7	W
Topr	Operation Temperature	-20 to +75	°C
Tstg	Storage Temperature	-25 to +125	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Units
		Min.	Typ.	Max.	
Vcc	Supply Voltage	4.5	5	5.5	V
fck	Clock Frequency		4	5	MHz



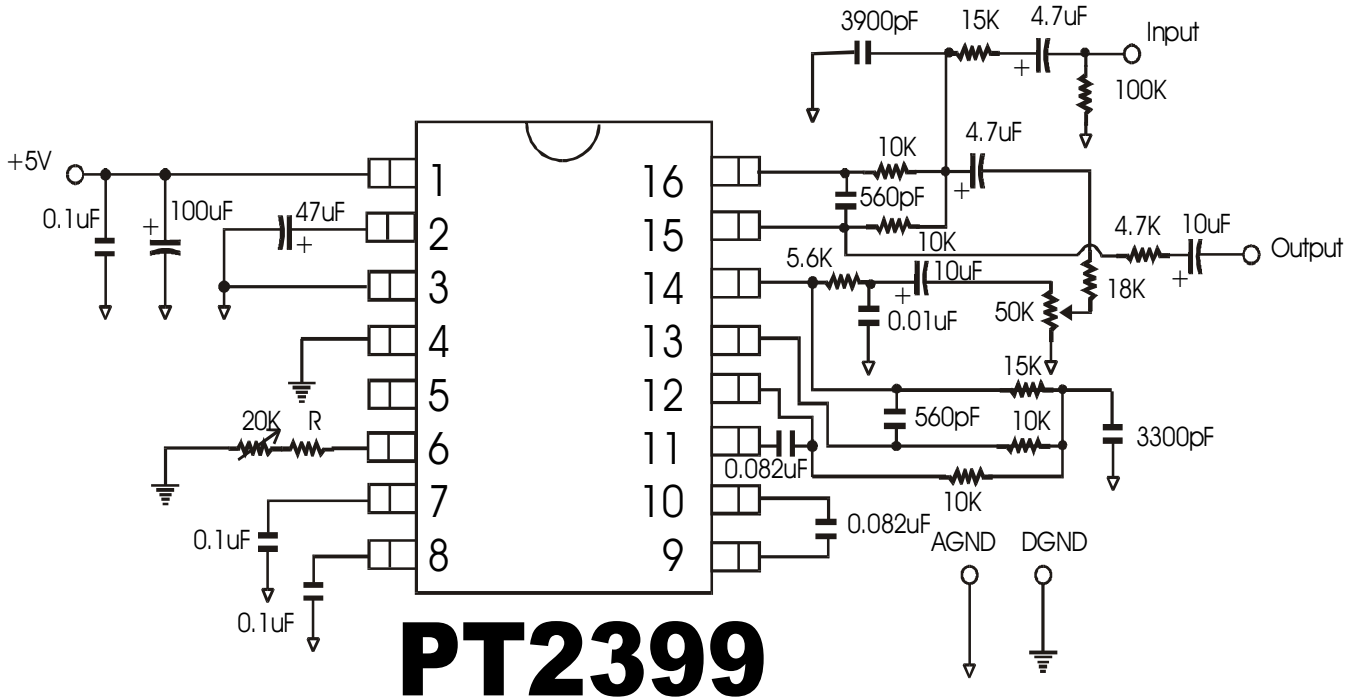
AC CHARACTERISTICS

(Unless otherwise stated: $V_{cc}=5.0\text{ V}$, $f_{in}=1\text{ KHz}$, $V_i=100\text{ mVrms}$, $f_{ck}=4\text{ MHz}$, $T_a=25^\circ\text{C}$)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{cc}	Supply Voltage		4.5	5.0	5.5	V
I_{cc}	Supply Current			30	40	mA
G_v	Voltage Gain	$R_L=47\text{ K Ohms}$		-0.5	2.5	dB
V_{omax}	Maximum Output Voltage	THD=10%	1.5	2	2.5	Vrms
THD	Output Distortion	filter=Audio		0.3	1.0	%
N_o	Output Noise Voltage	filter=A-weighting		-90	-80	dBV
PSRR	Power Supply Rejection Ratio	$\Delta V_{cc}=-20\text{ dBV}(0.1\text{ Vrms})$ $f=100\text{ Hz}$		-40	-30	dB



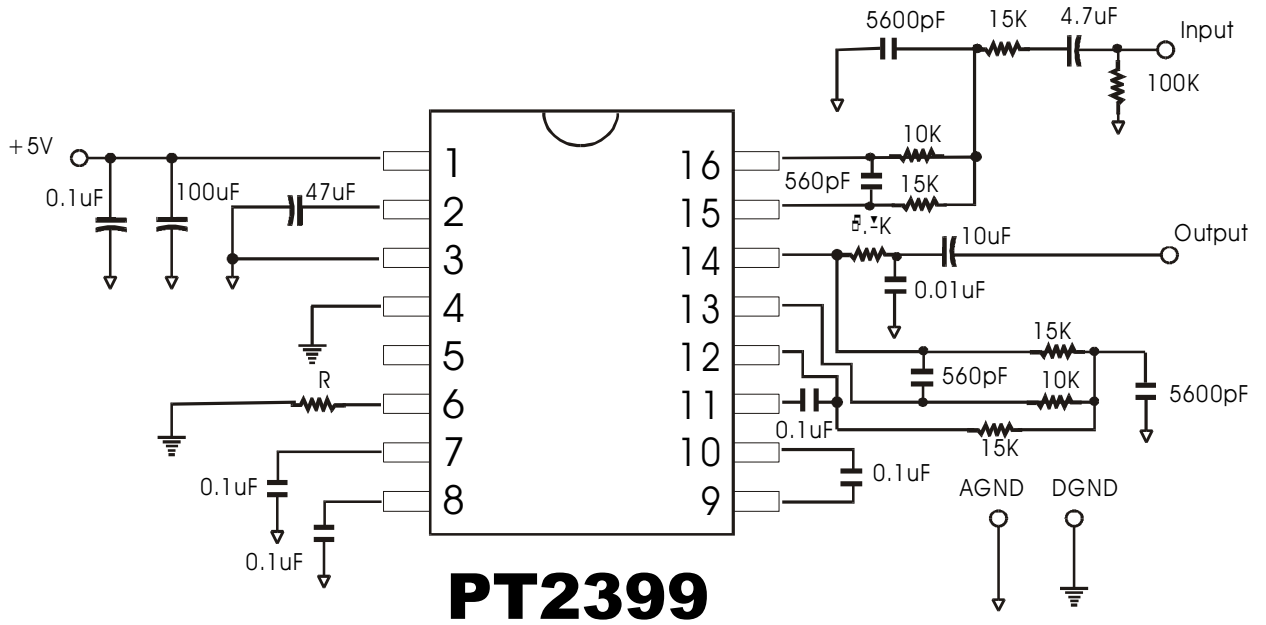
PT2399 ECHO APPLICATION CIRCUIT



Note: External Resistor having a value of 10 K Ohms to 50 K Ohms may be used. The recommended Resistor Value (R) is 10 K Ohms. When the value of the Resistor (R) increases, the range of the Delay Time also increases.



PT2399 SURROUND/DELAY APPLICATION CIRCUIT



Note: Please refer to Table 1 for the Resistor/Delay Time values



TABLE 1: RESISTOR/DELAY TIME VALUES

R	27.6K	21.3K	17.2K	14.3K	12.1K	10.5K	9.2K	8.2K
fck	2.0M	2.5M	3.0M	3.5M	4.0M	4.5M	5.0M	5.5M
td	342ms	273ms	228ms	196ms	171ms	151ms	136.6ms	124.1ms
THD	1.0%	0.8%	0.63%	0.53%	0.46%	0.41%	0.36%	0.33%

R	7.2K	6.4K	5.8K	5.4K	4.9K	4.5K	4K	3.4K
fck	6.0M	6.5M	7.0M	7.5M	8.0M	8.5M	9.0M	10M
td	113.7ms	104.3ms	97.1ms	92.2ms	86.3ms	81ms	75.9ms	68.1ms
THD	0.29%	0.27%	0.25%	0.25%	0.23%	0.22%	0.21%	0.19%

R	2.8K	2.4K	2K	1.67K	1.47K	1.28K	1.08K	894
fck	11M	12M	13M	14M	15M	16M	17M	18M
td	61.6ms	56.6ms	52.3ms	48.1ms	45.8ms	43ms	40.6ms	38.5ms
THD	0.18%	0.16%	0.15%	0.15%	0.15%	0.15%	0.14%	0.14%

R	723	519	288	0.5
fck	19M	20M	21M	22M
td	36.6ms	34.4ms	32.6ms	31.3ms
THD	0.14%	0.13%	0.13%	0.13%

Note: R = External Resistor (Ohms), please refer to PT2399 Surround/Delay Time Application Circuit
 fck = Clock Frequency (Hz)
 td = Delay Time
 THD = Total Harmonic Distortion

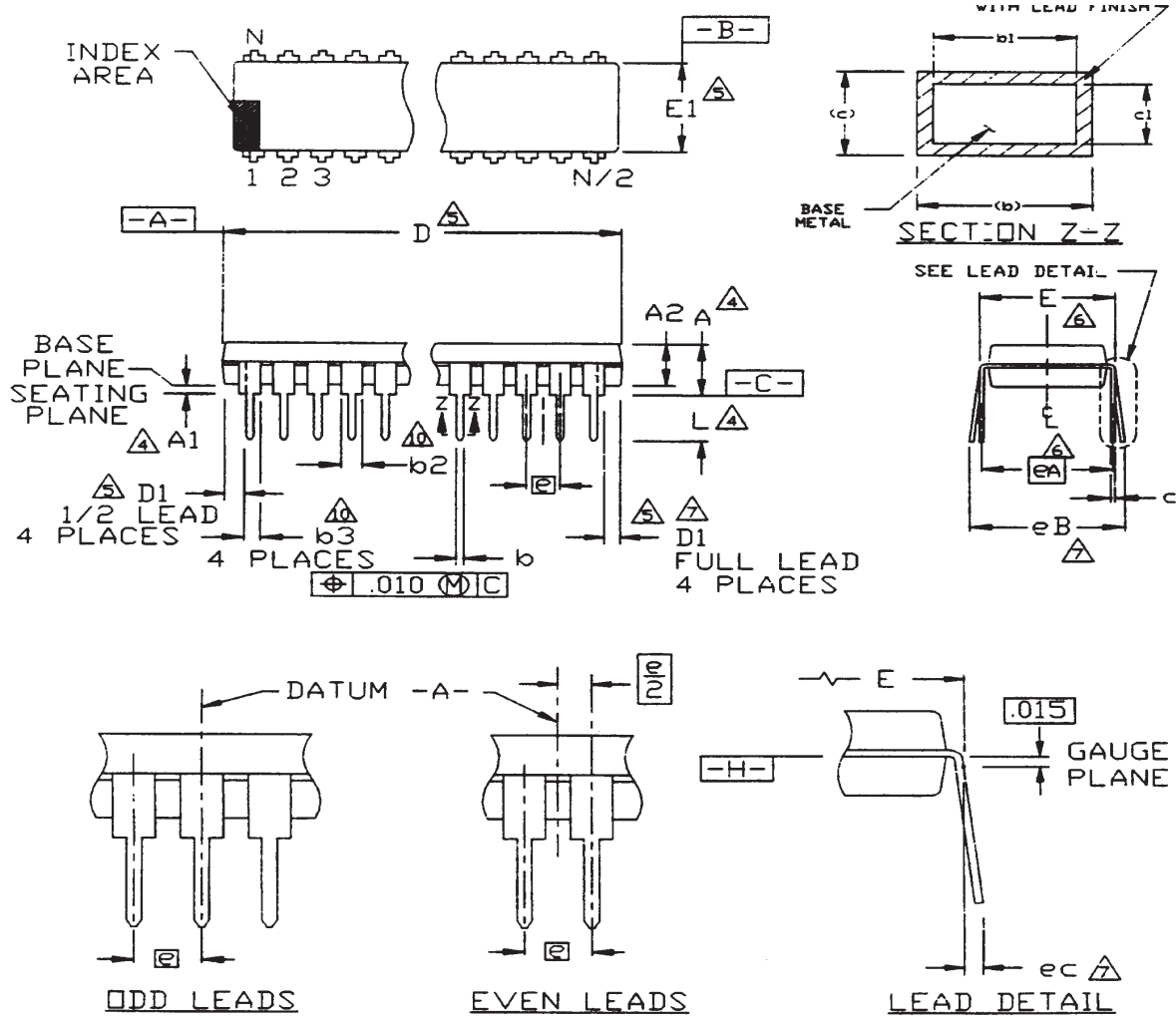


ORDER INFORMATION

Part Number	Package
PT2399	16 Pins, DIP (300 mil)
PT2399S	16 Pins, SO Package (300 mil)

PACKAGE INFORMATION

16 Pins, DIP Package (300 mil)





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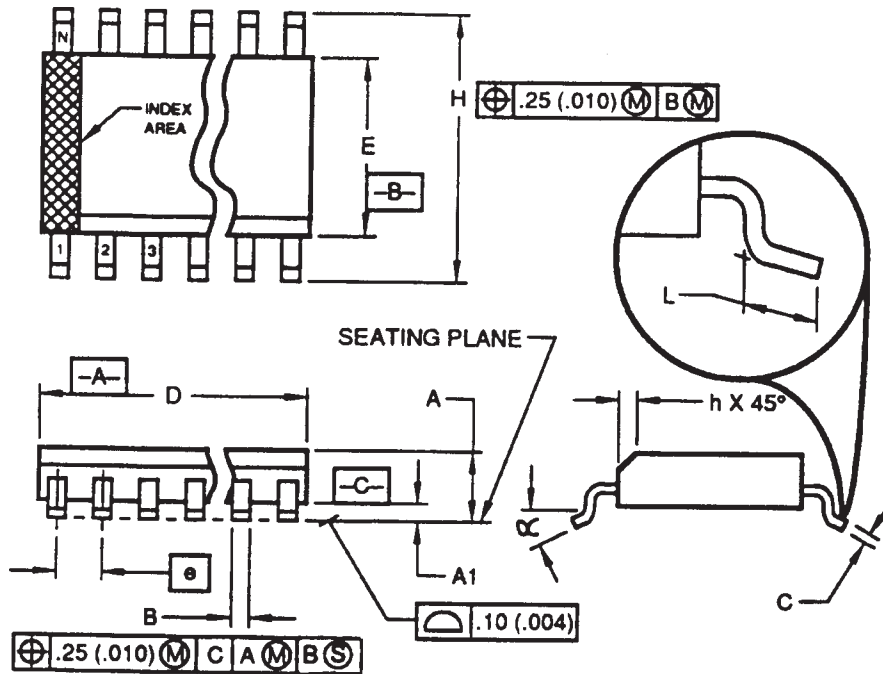
PT2399

Symbols	Dimensions in Inches		
	Min.	Nom.	Max.
A			0.210
A1	0.015		
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b1	0.014	0.018	0.020
b2	0.045	0.060	0.070
b3	0.030	0.039	0.045
c	0.008	0.010	0.014
c1	0.008	0.010	0.011
D	0.780	0.790	0.800
D1	0.005		
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e		0.100 bsc	
eA		0.300 bsc.	
eB			0.430
eC	0.000		0.060
L	0.115	0.130	0.150

- Notes:
1. All dimensions are in INCHES.
 2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
 3. Dimension "A", "A1" and "L" are measured with the package seated in JEDEC Seating Plane Gauge GS-3
 4. "D", "D1" and "E1" dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch.
 5. "E" and "eA" measured with the leads constrained to be perpendicular to datum -C- .
 6. "eB" and "eC" are measured at the lead tips with the leads unconstrained.
 7. N is the number of terminal positions (N=16)
 8. Pointed or rounded lead tips are preferred to ease insertion.
 9. "b2" and "b3" maximum dimensions are not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
 10. Distance between leads including Dambar protrusions to be 0.005 inch minimum.
 11. Datum plane -H- coincident with the bottom of lead, where lead exits body.
 12. Refer to JEDEC MS-001, Variation AB.



16 Pins, SO Package (300 mil)



Symbols	Dimensions in Millimeter		
	Min.	Nom.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D	10.10		10.50
E	7.40		7.60
e		1.27 bsc.	
H	10.00		10.65
h	0.25		0.75
L	0.40		1.27
α	0°		8°



Echo Processor IC

PT2399

- Notes:
1. Dimensioning and tolerancing per ANSI Y14.5-1982.
 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold Flash, protrusion or gate burrs shall not exceed 0.15mm (0.006 in) per side.
 3. Dimension "E" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm (0.010 in) per side.
 4. The chamfer on the body is optional. It is not present, a visual index feature must be located within the crosshatched area.
 5. "L" is the length of the terminal for soldering to a substrate.
 6. "N" is the number of terminal positions. (N=16)
 7. The lead width "B" as measured 0.36 mm (0.014 in) or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.24 in).
 8. Controlling dimension: MILLIMETER.
 9. Refer to JEDEC MS-013 Variation AA